Call for Papers

IEEE/ACM INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

November 5-9, 2018 • Hilton San Diego Resort & Spa, San Diego, CA • ICCAD.com

ORIGINAL TECHNICAL SUBMISSIONS ON, BUT NOT LIMITED TO, THE FOLLOWING TOPICS ARE INVITED:

1) SYSTEM-LEVEL CAD

1.1 System Design:
- System-level specification, modeling, and simulation
- System design flows and methods
- HW/SW co-design, co-simulation, co-optimization, and co-exploration
- HW/SW platforms for rapid prototyping
- System design case studies and applications
- System-level issues for 3D integration
- Micro-architectural transformation
- Memory architecture and system synthesis
- System communication architecture
- Network-on-chip design methodologies and CAD
- Network-on-chip design case studies and prototyping

1.2 Hardware for Embedded Systems :
- Multi-core/multi-processors systems
- HW/SW co-design for embedded systems
- Static and dynamic reconfigurable architectures
- Memory hierarchies and management
- System-level consideration of custom storage architectures (flash, phase change memory, STT-RAM, etc.)
- Application-specific instruction-set processors (ASIPs)

1.3 Neural Network and Neuromorphic Computing:
- Hardware and devices for neuromorphic and neural network computing
- Design method for learning on a chip
- Neural network acceleration techniques including GPGPU, FPGA and dedicated ASICs
- CAD for bio-inspired and neuromorphic systems

1.4 Embedded Systems Software and Software Security:
- Real-time software and operating systems
- Middleware and virtual machines, runtime support and resource management
- Timing analysis and WCET
- Profiling and compilation techniques, domain-specific embedded libraries
- Design exploration, synthesis, validation, verification, and optimization
- Software techniques and programming models for multicores, GPUs, and multithreaded embedded architectures
- System and embedded software security techniques
- Malware and Cloud security
- Security and privacy for the Internet of Things
- Embedded software forensics

1.5 Hardware Security
- Hardware-based security (CAD for PUF's, RNG, AES etc)
- Detection and prevention of hardware Trojans
- Side-channel attacks, fault attacks and countermeasures
- Split Manufacturing for security
- Design and CAD for security
- Security implications of CAD
- Cyberphysical system security
- Nanoelectronic security
- Supply chain security

1.6 Low Power and Approximate Computing in System Design
- Power and thermal estimation, analysis, optimization, and management techniques for hardware and software systems
- Energy- and thermal-aware application mapping and scheduling
- Energy- and thermal-aware dark silicon system design and optimization
- Energy- and thermal-aware architectures, algorithms and techniques
- Run-time management for the dark silicon
- New hardware techniques for approximate/stochastic computing

1.7 System Design Issues for Heterogeneous Computing
- Hardware-software partitioning of workloads
- Modeling and simulation of heterogeneous platforms
- High-level synthesis for heterogeneous computing
- Power/performance analysis of heterogeneous and cloud platforms
- Programming environment of heterogeneous computing
- Application driven heterogeneous platforms for big data, machine learning etc.
- Cloud Internet-of-Things (IoT) applications
- Interaction of Internet-of-Things (IoT) devices and the cloud
- Cloud computation for Internet-of-Things (IoT) devices
- Applications and designs for systems based on optical devices

2) SYNTHESIS, VERIFICATION, AND PHYSICAL DESIGN

2.1 High-Level, Behavioral, and Logic Synthesis and Optimization:
- High-level/Behavioral/Logic synthesis
- Technology-independent optimization and technology mapping
- Functional and logic timing ECO
- Resource scheduling, allocation, and synthesis
- Interaction between logic synthesis and physical design

2.2 Testing, Validation, Simulation, and Verification:
- High-level/Behavioral/Logic modeling and validation
- High-level/Behavioral/Logic synthesis
- Formal, semi-formal, and assertion-based verification
- Equivalence and property checking
- Emulation and hardware simulation/acceleration
- Post-silicon functional validation
- Digital fault modeling and simulation
- Delay, current-based, low-power test
- ATPG, BIST, DFT, and compression
- Memory test and repair
- Core, board, system, and 3D IC test
- Post-silicon validation and debug
- Analog, mixed-signal, and RF test

2.3 Cell-Library Design, Partitioning, Floorplanning, Placement:
- Cell-library design and optimization
- Transistor and gate sizing
- High-level physical design and synthesis
- Estimation and hierarchy management
- 2D and 3D partitioning, floorplanning, and placement
- Post-placement optimization
- Buffer insertion and interconnect planning

2.4 Clock Network Synthesis, Routing, and Post-Layout Optimization and Verification:
- 2D and 3D clock network synthesis
- 2D and 3D global and detailed routing
- Package-/Board-level routing and chip-package-board co-design
- Post-layout/-silicon optimization
- Layout and routing issues for optical interconnects

3) SOC ANALYSIS, DESIGN, SIMULATION, AND TESTING

3.1 Design for Manufacturability:
- Process technology characterization, extraction, and modeling
- CAD for design/manufacturing interfaces
- CAD for reticle enhancement and lithography-related design
- Variability analysis and statistical design and optimization
- Yield estimation and design for yield
- Physical verification and design rule checking
- DFM for emerging devices (3D, nanophotonics, non-volatile logic/memory, etc.)
- Machine learning for smart manufacturing and process control

3.2 Design for Reliability:
- Analysis and optimization for device-level reliability issues (stress, aging effects, ESD, etc.)
- Analysis optimization for interconnect reliability issues (electromigration, thermal, etc.)
- Reliability issues related to soft errors
- Design for resilience and robustness
- Reliability issues for emerging devices (3D, optical, non-volatile, etc.)

3.3 Timing, Power and Signal Integrity Analysis and Optimization
- Deterministic and statistical static timing analysis and optimization
- Power and leakage analysis and optimization
- Circuit and interconnect-level low power design issues
- Power/ground network analysis and synthesis
- Signal integrity analysis and optimization

3.4 CAD for Analog/Mixed-Signal/RF and Multi-Domain Modeling
- CAD for analog, mixed-signal, RF
- CAD for mixed-domain (semiconductor, nanoelectronic, MEMS, and electro-optical) devices, circuits, and systems
- CAD for nanophotonics and optical devices
- Analog, mixed-signal, and RF noise modeling and simulation
- Device, interconnect and circuit extraction and simulation
- Package modeling and analysis
- EM simulation and optimization
- Behavior modeling of devices and interconnect
- Modeling of complex dynamical systems (molecular dynamics, fluid dynamics, computational finance, etc.)

4) CAD FOR EMERGING TECHNOLOGIES, PARADIGMS, AND APPLICATIONS

4.1 Biological Systems and Electronics, Brain Inspired Computing, and New Computing Paradigms:
- CAD for biological computing systems
- CAD for systems and synthetic biology
- CAD for bio-electronic devices, bio-sensors, MEMS, and systems

4.2 Nanoscale and Post-CMOS Systems:
- New device structures and process technologies
- New memory technologies (flash, phase change memory, STT-RAM, memristor, etc.)
- Nanotechnologies, nanowires, nanotubes, graphene, etc.
- Quantum computing
- Optical devices, computing, and communication

4.3 CAD for Cyber-Physical Systems:
- CAD for Internet-of-Things (IoT) and sensor networks
- Design issues for Internet-of-Things (IoT) Devices
- Modeling and analysis of CPS
- CAD for automotive systems and power electronics
- Dependable and safe CPS design
- Analysis and optimization of data centers
- CAD for display electronics
- Green computing (smart grid, energy, solar panels, etc.)

Call for Papers

DEADLINE FOR ELECTRONIC SUBMISSION OF ABSTRACTS:
Monday, April 16, 2018 • 5:00pm Pacific Daylight Time (GMT-7)

DEADLINE FOR ELECTRONIC SUBMISSION OF PAPERS:
Monday, April 23, 2018 • 5:00pm Pacific Daylight Time (GMT-7)

SUBMISSION DETAILS

Paper submissions must be made through the online submission system at the ICCAD web site: **https://www.softconf.com/i/iccad2018.**

Regular papers will be reviewed as finished papers; preliminary submissions will be at a disadvantage.

Authors are asked to submit their work in two stages. In stage one (abstract submission), a title, abstract, and a list of all co-authors must be submitted via the ICCAD web submission site. In stage two (paper submission), the paper itself is submitted. Authors are responsible for ensuring that their paper submission meets all guidelines, and that the PDF is readable.

DEADLINE FOR ABSTRACT SUBMISSIONS

The submission abstract deadline is **5:00 pm Pacific Daylight Time (GMT -07:00), Monday April 16, 2018.** No abstract submissions will be possible after this deadline.

DEADLINE FOR PAPER SUBMISSIONS

The submission paper deadline is **5:00 pm Pacific Daylight Time (GMT -07:00), Monday April 23, 2018.**

We always have several authors contact the ICCAD office asking for a deadline extension. Due to the limited review cycle, NO extensions are granted for ANY reason.

REGULAR PAPER SUBMISSIONS

- All papers must be in PDF format only, with savable text.
- Each paper must be no more than 8 pages (including the abstract, figures, tables, and references), double-columned, 9pt or 10pt font.
- Your submission must not include information that serves to identify the authors of the manuscript, such as name(s) or affiliation(s) of the author(s), anywhere in the manuscript, abstract, or in the embedded PDF data. References and bibliographic citations to the author(s) own published works or affiliations should be made in the third person.
- Submissions not adhering to these rules, or determined to be previously published (this includes pre-prints publicly available on personal or other websites, such as arXiv, or publicly available internal memoranda with author names divulged) or simultaneously submitted to another conference, or journal, will be summarily rejected. Internal memoranda with full content not publicly available, and with author names not divulged, may be submitted.

IMPORTANT: Final camera-ready versions must be identical to the submitted papers with the following exceptions; inclusion of author names/affiliation, correction of identified errors, addressing reviewer-demanded changes. No other modifications of any kind are allowed including modification of title, change of the author list, reformatting, restyling, rephrasing, removing figures/results/text, etc. The TPC Chairs reserve the right to finally reject any manuscripts not adhering to these rules. A report detailing all the revisions made must be submitted together with the final camera-ready manuscript once any revision is conducted.

TEMPLATES

Paper templates are available at the ICCAD website; authors are recommended to format their papers based on the templates.

NOTIFICATION OF ACCEPTANCE

Authors will be notified of acceptance on or before **Wednesday, June 27, 2018.** Final paper guidelines will be sent at that time.

PROCEEDINGS

The deadline for final papers is **Wednesday, July 25, 2018.** Accepted papers are allowed six pages in the conference proceedings free of charge. Each additional page beyond six pages is subject to the page charge at $150.00 per page up to the eight-page limit. IEEE will hold the copyright for ICCAD 2018 proceedings. Authors of accepted papers must sign an IEEE copyright release form for their paper.

CONFERENCE REGISTRATION

At least one author per accepted paper must register by **Friday, August 31, 2018,** at the discounted speaker's registration rate. Failure to register will result in your paper being removed from the conference proceedings. IEEE reserves the right to exclude a paper from distribution after the conference (e.g., removal from IEEE Xplore) if the paper is not presented at the conference.

ACM/IEEE WILLIAM J. MCCALLA ICCAD BEST PAPER AWARDS

Two papers, one from front-end and one from back-end, will be awarded with this prestigious award. The winners will be chosen from nominated papers after a thorough and competitive process by area-specific selection committees and announced at the opening session.

ICCAD TEN-YEAR RETROSPECTIVE MOST INFLUENTIAL PAPER AWARD

One paper from 2008 and 2009 editions of ICCAD will be selected for this outstanding recognition as evidenced by impact on the research community reflected in citations, on the vendor community via its use in an industrial setting, or by initiating new research venues during the past decade. Nominations from the community are welcome and can be sent to Yuan Xie, Technical Program Vice-Chair at **yuanxie@ece.ucsb.edu.**

CALL FOR WORKSHOP, TUTORIAL, SPECIAL SESSION, PANEL AND KEYNOTE PROPOSALS ALL DUE THURSDAY, APRIL 26, 2018.

Please visit **ICCAD.com** for complete details.

ICCAD serves EDA and design professionals, highlighting new challenges and innovative solutions for Integrated Circuit Design Technologies and Systems. ICCAD covers the full range of CAD topics – from device and circuit-level CAD up through system-level CAD and embedded software, as well as CAD for post-CMOS design and novel application areas, such as biology and nanotechnology.

In cooperation with:

Call for Proposals

PROPOSALS

*CALL FOR WORKSHOP, TUTORIAL, SPECIAL SESSION, PANEL AND KEYNOTE PROPOSALS, ALL DUE **THURSDAY, APRIL 26, 2018.***

WORKSHOP PROPOSALS

ICCAD provides a vibrant and supportive environment for small-to-medium-sized affiliated workshops. Typical workshops are one-day events on the Thursday of ICCAD, with ICCAD providing all logistical support (registration, lunch, room bookings, hotel, pre-conference financials, etc.)

All workshop proposals should be sent to Tulika Mitra, Workshop Chair, at **tulika@comp.nus.edu.sg.**

TUTORIAL PROPOSALS

All ICCAD tutorials are embedded in the main technical program and free to conference attendees, providing value to attendees and a good audience for presenters. Typical tutorials run 1.5-2 hours, although longer tutorials (consisting of two session blocks of 1.5-2 hours each) may be considered. Tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and must include a list of suggested participants with biographical data. Proposals should focus on the state-of-the-art in a specific area of broad interest amongst ICCAD attendees. All tutorial proposals should be sent to Rolf Drechsler, Tutorial and Special Session Chair, at **drechsler@uni-bremen.de**.

SPECIAL SESSION PROPOSALS

Special Sessions typically run 1.5-2 hours. Special session proposals should focus on in-depth treatment on a topic of timely interest to the ICCAD audience. Special session proposals should not exceed two pages, should describe the topic and intended audience, and must include a list of suggested participants with biographical data. All special session proposals should be sent to Rolf Drechsler, Tutorial and Special Session Chair, at **drechsler@uni-bremen.de.**

PANEL PROPOSALS

Panel suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Panel suggestions must include a bulleted outline of covered topics. All panel proposals should be sent to David Pan, Technical Program Chair at **dpan@ece.utexas.edu**.

KEYNOTE PROPOSALS

Keynote proposals should include descriptions of suggested keynote speakers, and the importance of the speech to the ICCAD audience. All keynote proposals should be sent to Iris Bahar, General Chair, at **iris_bahar@brown.edu.**

ICCAD reserves the right to restructure all panel, special session, and tutorial proposals.

IF YOU NEED ASSISTANCE, PLEASE CONTACT THE APPROPRIATE COMMITTEE MEMBERS:

General Chair:
Iris Bahar, **iris_bahar@brown.edu**

Program Chair:
David Pan, **dpan@ece.utexas.edu**

Vice Program Chair:
Yuan Xie, **yuanxie@ece.ucsb.edu**

Tutorial and Special Session Chair:
Rolf Drechsler, **drechsler@uni-bremen.de**

Workshop Chair:
Tulika Mitra, **tulika@comp.nus.edu.sg**

In cooperation with: