

Monday, November 10, 2003

ICCAD-2003

Registration - 7:00 AM - 6:00 PM (Bayshore Foyer)

Continental Breakfast - 7:00 AM (Sierra/Cascade Ballroom)

Speakers' Breakfast - 7:30 AM (Monterey Room)

8:30	OPENING SESSION & KEYNOTE ADDRESS: CMOS, SCALING, AND THE FUTURE Mark Horowitz - Professor, Stanford Univ., Stanford, CA (Pine/Fir Ballroom)			
9:45	Coffee Break			
	Cedar Ballroom	Pine/Fir Ballroom	Donner/Siskiyou Ballroom	Oak Ballroom
10:30	SESSION 1A	SESSION 1B	SESSION 1C	SESSION 1D
	Interconnect-Centric SoC Design	Energy Optimization using Dynamic Voltage Scaling for Embedded Systems	New Opportunities in High-Level Synthesis	New Ideas in Placement and Floorplanning
12:00	12:00 - 2:00 Lunch Break (Sierra/Cascade Ballroom)			
12:30				
2:00	SESSION 2A	SESSION 2B	SESSION 2C	
	Improvements in SoC Testing	Electrical and Power Models - System to Transistor Level	Embedded Tutorial: Design and CAD Challenges for Sub-90nm CMOS Technology (Donner/Siskiyou Ballroom)	
3:30	Coffee Break			
4:00	SESSION 3A	SESSION 3B	SESSION 3C	SESSION 3D
	Emerging Techniques in Dynamic Verification	Delay and Signal Modeling for Timing Analysis	Software Techniques for Energy and Performance Optimization in Embedded Systems	Optimization of Global Interconnects
6:00				

ICCAD BioGarten (in the Gateway Foyer) • 6:00 PM - 6:30 PM

MONDAY NIGHT PANEL: SEMICONDUCTOR SLOWDOWN: WHO WILL BLINK FIRST?

6:30 PM - 8:00 PM
(Pine/Fir Ballroom)

ICCAD-2003

Tuesday, November 11, 2003

Registration - 7:00 AM - 6:00 PM (Bayshore Foyer)

Continental Breakfast - 7:00 AM (Sierra/Cascade Ballroom)

Technology Fair - 10:00 AM - 7:00 PM (Gateway Foyer)

Speakers' Breakfast - 7:30 AM (Monterey Room)

Cedar Ballroom	Pine/Fir Ballroom	Donner/Siskiyou Ballroom	Oak Ballroom	
SESSION 4A	SESSION 4B	SESSION 4C	SESSION 4D	8:30
Numerical Methods for Analog Optimization and Analysis	CAD Algorithms for Emerging Technologies	Design Techniques for Customized Processors	New Improvements in Placement	10:00
Coffee Break				
SESSION 5A	SESSION 5B	SESSION 5C	SESSION 5D	10:30
Optimizations for Verification Engines	System Design Concepts	Analog Design and Methodology	Routing	12:00
12:00 - 2:00 Lunch Break (Sierra/Cascade Ballroom)				
SESSION 6A	SESSION 6B	SESSION 6C	SESSION 6D	2:00
Automatic Abstraction for Formal Verification	Embedded Tutorial: System Level Design and Verification using a Synchronous Language	Nonlinear Modelling of Analog and Optical Systems	Timing and Tradeoffs in Placement	3:30
Coffee Break				
SESSION 7A	SESSION 7B	SESSION 7C	SESSION 7D	4:00
Simulation at the Nanometer Scale	Energy Issues in System Design	Constraint Driven High-Level Synthesis	Optimal Interconnect Synthesis and Analysis	6:00
DINNER 6:30 PM • Flamenco performance following dinner. (Sierra/Cascade Ballroom)				

Wednesday, November 12, 2003

ICCAD-2003

Registration - 7:00 AM - 6:00 PM (Bayshore Foyer) Continental Breakfast - 7:00 AM (Sierra/Cascade Ballroom) Speakers' Breakfast - 7:30 AM (Monterey Room)

	Cedar Ballroom	Pine/Fir Ballroom	Donner/Siskiyou Ballroom	Oak Ballroom
8:30	SESSION 8A Memory Testing	SESSION 8B Statistical Static Timing - I	SESSION 8C Power-Aware Design	SESSION 8D Interconnect Reduction
10:00	Coffee Break			
10:30	SESSION 9A Embedded Tutorial: Mixed Signal DFT: A Concise Overview	SESSION 9B Embedded Tutorial: Manufacturing-Aware Physical Design	SESSION 9C Cool Topics in Logic Synthesis	SESSION 9D Graph Algorithmic Approaches to EDA Problems
12:00	12:00 - 2:00 Lunch Break (Sierra/Cascade Ballroom)			
12:30	12:00 - 2:00 Lunch Break (Sierra/Cascade Ballroom)			
2:00	SESSION 10A Parametric Considerations in Test Schemes	SESSION 10B Power-Grid and Substrate Analysis	SESSION 10C Hot Topics in Logic Synthesis	SESSION 10D Interconnect Modeling
4:00	Coffee Break			
4:30	SESSION 11A Test Data Reduction Techniques	SESSION 11B Embedded Tutorial: Formal Methods for Dynamic Power Management	SESSION 11C Embedded Tutorial: Large- Scale Circuit Placement: Gap and Promise	SESSION 11D Statistical Static Timing - II
6:00	ICCAD BierGarten (in the Gateway Foyer) 6:00PM-6:30PM			

• See you next year! November 7 - 11, 2004

Tutorials9:00 AM - 5:00 PM	Registration8:00 AM - 10:00 AM
Continental Breakfast8:00 AM - 9:00 AM	Lunch12:00 PM - 1:00 PM

Registration Fees

IEEE/ACM Member	\$360.00
Non-Member	\$450.00
IEEE/ACM Student	\$220.00

Tutorial 1 - Linux for EDA

Cedar Ballroom

- Speakers: Stephen Edwards - *Columbia Univ., New York, NY*
 Tom Grotton - *Cadence Design Systems, Inc., San Jose, CA*
 Tim Marriott - *Synopsys, Inc., Santa Clara, CA*
 Mel Nicholson - *Synopsys, Inc., Santa Clara, CA*
 Fabio Somenzi - *Univ. of Colorado, Boulder, CO*

Tutorial 2 - Leakage Issues in IC Design: Trends, Estimation and Avoidance

Pine Ballroom

- Speakers: Siva Narendra - *Intel Labs., Hillsboro, OR*
 David Blaauw - *Univ of Michigan, Ann Arbor, MI*
 Anirudh Devgan - *IBM Research, Austin, TX*
 Farid Najm - *Univ. of Toronto, Toronto, ON, Canada*

Tutorial 3 - Recent Advances in Formal Verification

Fir Ballroom

- Speakers: Pei-Hsin Ho - *Synopsys, Inc., Beaverton, OR*
 Ken McMillan - *Cadence Berkeley Labs., Berkeley, CA*
 Vigyan Singhal - *Jasper Design Automation, Inc., Fremont, CA*

Tutorial 4 - Embedded Software Development

Oak Ballroom

- Speakers: Lance Brooks - *Mentor Graphics Corp., Mobile, AL*
 Michael McGrath - *Intel Corp., Chandler, AZ*
 Vladimir Ivanovic - *California State Univ., Hayward, CA*

Opening Session

Monday, November 10, 2003 • 8:30 AM
Pine/Fir Ballroom

Opening Remarks

Andreas Kuehlmann - ICCAD-2003 General Chair, Cadence
Berkeley Labs., Berkeley, CA

Hidetoshi Onodera - ICCAD-2003 Program Chair, Kyoto Univ.,
Kyoto, Japan

Award Presentations

IEEE/ACM William J. McCalla ICCAD Best Paper Award

This award is given in memory of William J. McCalla, for his contributions to ICCAD and his CAD technical work through his career.

Paper 6C.1 - Noise Analysis for Optical Fiber Communication Systems

Alper Demir - KOC University, Sariyer-Istanbul, Turkey

Paper 8B.1 - Block-Based Static Timing Analysis with Uncertainty

Anirudh Devgan - IBM Research, Austin, TX

Chandramouli Kashyap - IBM Microelectronics, Austin, TX

CAS Industrial Pioneer Award

Prabhu Goel - iPolicy Networks, Inc., Fremont, CA

For his contributions to design modeling and design verification through Verilog and Verilog based design tools that dramatically boosted the productivity of design engineers. Presented by:

Giovanni De Micheli, IEEE CAS Society President

2003 SIGDA Outstanding New Faculty Award

Dennis Sylvester - Univ. of Michigan, Ann Arbor, MI

The SIGDA Outstanding New Faculty Award recognizes a junior faculty member early in her or his academic career who demonstrates outstanding potential as an educator and researcher in the field of electronic design automation. The award is presented annually at ICCAD, and consists of a \$10,000 grant supporting the faculty member's research program, as well as a citation.

Presented by: Robert Walker, ACM/SIGDA Chair

Nikil Dutt, ACM/SIGDA Advisory Board

ACM/SIGDA CADathlon Award

Awards will be presented to the winners of the Sunday programming contest. Presented by: Robert Walker, ACM/SIGDA Chair

Soha Hassoun, ACM/SIGDA Advisory Board

2002-2003 ACM Outstanding Ph.D. Dissertation Award in Electronic Design Automation

Luca Daniel - Univ. of California, Berkeley, CA

For his dissertation entitled "*Simulation and Modeling Techniques for Signal Integrity and Electromagnetic Interference on High Frequency Electronic Systems*".

Lintao Zhang - Princeton University, Princeton, NJ

For his dissertation entitled "*Searching for Truth: Techniques for Satisfiability of Boolean Formulas*".

Presented by: Robert Walker, ACM/SIGDA Chair

Massoud Pedram, ACM/SIGDA Advisory Board

Keynote

CMOS, Scaling, and The Future

Mark Horowitz - Professor, Stanford Univ., Stanford, CA

Keynote Address

ICCAD-2003

International Conference on Computer Aided Design

Keynote: **CMOS, Scaling, and the Future**

Mark Horowitz - Professor, Stanford Univ., Stanford, CA

8:30 AM - 9:45 AM

Room: Pine/Fir Ballroom

Technology scaling has driven integrated circuit designers for the past four decades, both enabling them to create ever more complex electronic systems, but also forcing them to change the way that they think about design. This talk is a mostly serious look at the factors driving designers today, looking at design issues that future designers will need to face.

Although technology scaling is a predictable and smooth process, designer's response is not smooth, and often has step-like changes when new tools or techniques are introduced. Some of the most dramatic design changes occur when the basic circuit technology changes, but other design changes can be as large, like the introduction of HDL and synthesis. We are currently facing a number of issues which might lead to large changes in design. The most critical is power. Previous shifts in circuit style, from bipolar (TTL and ECL, if you are old enough to remember) to nMOS, and then from nMOS to the CMOS style we have been using for roughly the past 20 years were partially driven by power issues. Yet today's CMOS chips dissipate more power than even the old bipolar chips did, and the scaling trends are not promising. The looming power constraints will force us to worry about performance efficiency instead of performance, since in the future the peak performance solution will always dissipate too much power.

Biography: Mark Horowitz is the Yahoo Founder's Professor of Electrical Engineering and Computer Science at Stanford University. He received his BS and MS in Electrical Engineering from MIT in 1978, and his PhD from Stanford in 1984. Dr. Horowitz is the recipient of a 1985 Presidential Young Investigator Award, and an IBM Faculty Development Award, as well as the 1993 Best Paper Award at the International Solid State Circuits Conference.

Dr. Horowitz's research area is in digital system design, and he has led a number of processor designs including MIPS-X, one of the first processors to include an on-chip instruction cache, TORCH, a statically-scheduled, superscalar processor that supported speculative execution, and FLASH, a flexible DSM machine. He has also worked in a number of other chip design areas including high-speed and low-power memory design, high-bandwidth interfaces, and fast floating point. In 1990 he took leave from Stanford to help start Rambus Inc., a company designing high-bandwidth chip interface technology. His current research includes multiprocessor design, low power circuits, memory design, and high-speed links.

Time: 10:30 AM to 12:00 PM

Room: Cedar

SESSION 1A INTERCONNECT-CENTRIC SOC DESIGN

Moderators: Kaustav Banerjee - *Univ. of California, Santa Barbara, CA*
Tajana Simunic - *Hewlett-Packard Labs./Stanford Univ., Palo Alto, CA*

Three on-chip interconnect designs are presented. The first explores dynamically varying the error protection scheme to maintain constant BER while minimizing energy consumption. The second presents a highly-scalable bus architecture for system-on-chip. The third analytically quantifies the throughput and implementation details of the Y-interconnect approach.

1A.1 ADAPTIVE ERROR PROTECTION FOR ENERGY EFFICIENCY

Lin Li (lili@cse.psu.edu), N. Vijaykrishnan, Mahmut Kandemir, Mary Jane Irwin - *Penn State Univ., University Park, PA*

1A.2 SAMBA-BUS: A HIGH PERFORMANCE BUS ARCHITECTURE FOR SYSTEM-ON-CHIPS

Ruibing Lu (lur@ecn.purdue.edu), Cheng-Kok Koh - *Purdue Univ., West Lafayette, IN*

1A.3 THE Y-ARCHITECTURE FOR ON-CHIP INTERCONNECT: ANALYSIS AND METHODOLOGY

Hongyu Chen, Chung-Kuan Cheng, Andrew B. Kahng, Ion Mandoiu, Qinke Wang (qiwang@cs.ucsd.edu) - *Univ. of California at San Diego, La Jolla, CA*

SESSION 1B ENERGY OPTIMIZATION USING DYNAMIC VOLTAGE SCALING FOR EMBEDDED SYSTEMS

Moderators: Stan Y. Liao - *Synopsys, Inc., Mountain View, CA*
Hiroyuki Tomiyama - *Nagoya Univ., Nagoya, Japan*

Dynamic voltage scaling promises significant energy reduction in embedded systems. This session presents a number of system-level approaches to dynamically assigning voltages. The first paper uses network flow to produce optimal assignments of processes to a small predefined set of voltages. The second paper derives analytical solutions for the voltage set-up problem. The third paper combines dynamic voltage scaling with adaptive body biasing for minimizing leakage power.

1B.1 GENERALIZED NETWORK FLOW TECHNIQUES FOR DYNAMIC VOLTAGE SCALING IN HARD-REAL-TIME SYSTEMS

Vishnu Swaminathan (vishnus@ee.duke.edu), Krishnendu Chakrabarty - *Duke Univ., Durham, NC*

1B.2 APPROACHING THE MAXIMUM ENERGY SAVING ON EMBEDDED SYSTEMS WITH MULTIPLE VOLTAGES

Shaoyong Hua (shua@glue.umd.edu), Gang Qu - *Univ. of Maryland, College Park, MD*

1B.3 COMBINED DYNAMIC VOLTAGE SCALING AND ADAPTIVE BODY BIASING FOR HETEROGENEOUS DISTRIBUTED REAL-TIME EMBEDDED SYSTEMS

Le Yan (lyan@ee.princeton.edu), Jiong Luo, Niraj K. Jha - *Princeton Univ., Princeton, NJ*

7 Time: 10:30 AM to 12:00 PM

Room: Pine/Fir

Time: 10:30 AM to 12:30 PM

Room: Donner/Siskiyou

SESSION 1C NEW OPPORTUNITIES IN HIGH-LEVEL SYNTHESIS

Moderators: James C. Hoe - *Carnegie Mellon Univ., Pittsburgh, PA*
Steve Haynal - *Intel Corp., Hillsboro, OR*

This session presents four new ideas that leverage information in high-level synthesis (HLS). The first paper extracts opportunities for power optimization during HLS to assist transformations at the gate-level. The second analyzes an application's memory access pattern to synthesize an efficient partitioned memory architecture. The third uses available timing slack in scheduling to improve timing closure. The final paper explores synthesis for a new dynamic threaded hardware.

- 1C.1 **RTL POWER OPTIMIZATION WITH GATE LEVEL ACCURACY**
Qi Wang (qwang@cadence.com) - *Cadence Design Systems, Inc., San Jose, CA*
Sumit Roy - *Calypto Design Systems, Inc., San Jose, CA*
- 1C.2 **SYNTHESIS OF HETEROGENEOUS DISTRIBUTED ARCHITECTURES FOR MEMORY-INTENSIVE APPLICATIONS**
Chao Huang (chaoh@ee.princeton.edu) - *Princeton Univ., Princeton, NJ*
Srivaths Ravi, Anand Raghunathan - *NEC Labs., Princeton, NJ*
Niraj K. Jha - *Princeton Univ., Princeton, NJ*
- 1C.3 **ACHIEVING DESIGN CLOSURE THROUGH DELAY RELAXATION PARAMETER**
Ankur Srivastava (ankurs@glue.umd.edu) - *Univ. of Maryland, College Park, MD*
Seda Ogrenci Memik, Bo-Kyung Choi, Majid Sarrafzadeh - *Univ. of California, Los Angeles, CA*
- 1C.4 **HARDWARE SCHEDULING FOR DYNAMIC ADAPTABILITY USING EXTERNAL PROFILING AND HARDWARE THREADING**
Brian G. Swahn (swahn@ece.tufts.edu), Soha Hassoun - *Tufts Univ., Medford, MA*

Time: 10:30 AM to 12:30 PM

Room: Oak

SESSION 1D NEW IDEAS IN PLACEMENT AND FLOORPLANNING

Moderators: David Z. Pan - *Univ. of Texas, Austin, TX*
Kia Bazargan - *Univ. of Minnesota, Minneapolis, MN*

This session deals with new approaches to placement and floorplanning. The first paper deals with an integrated approach to bus planning and floorplanning. The second paper introduces new methods for creating wire and area-optimized floorplans. The third paper deals with the idea of improving predictability, robustness and performance in placement. The final paper deals with a new approach to thermal placement.

- 1D.1 **BUS-DRIVEN FLOORPLANNING**
Hua Xiang (huaxiang@uiuc.edu) - *Univ. of Illinois, Urbana, IL*
Xiaoping Tang - *Cadence Design Systems, Inc., San Jose, CA*
Martin D. F. Wong - *Univ. of Illinois, Urbana, IL*
- 1D.2 **A NOVEL GEOMETRIC ALGORITHM FOR FAST WIRE OPTIMIZED FLOORPLANNING**
Peter G. Sassone, Sung K. Lim (limsk@ece.gatech.edu) - *Georgia Institute of Tech., Atlanta, GA*
- 1D.3 **PLACEMENT METHOD TARGETING PREDICTABILITY, ROBUSTNESS AND PERFORMANCE**
Cristinel Ababei (ababei@ece.umn.edu), Kia Bazargan - *Univ. of Minnesota, Minneapolis, MN*
- 1D.4 **EFFICIENT THERMAL PLACEMENT OF STANDARD CELLS IN 3D ICs USING A FORCE DIRECTED APPROACH**
Brent A. Goplen (bgoplen@ece.umn.edu), Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

Time: 2:00 PM to 3:30 PM

Room: Cedar

SESSION 2A IMPROVEMENTS IN SOC TESTING

Moderators: Bozena Kaminska - *3rd Millennium Test Solutions, Lake Oswego, OR*
Krishnendu Chakrabarty - *Duke Univ., Durham, NC*

Core-based design boosts productivity but imposes numerous test challenges. Effective test integration in the face of Intellectual Property preservation constraints is addressed in the first paper. While considerable work has already been performed in digital SOC wrapper design, integrating analog cores in mixed-signal SOC's necessitates novel approaches, an area addressed by the second paper. The session concludes with a paper on SOC test scheduling capable of considering test power constraints.

- 2A.1 PARTIAL CORE ENCRYPTION FOR PERFORMANCE-EFFICIENT TEST OF SOC's
Ozgur Sinanoglu (ozgur@cs.ucsd.edu), Alex Orailoglu - *Univ. of California at San Diego, La Jolla, CA*
- 2A.2 TAM OPTIMIZATION FOR MIXED-SIGNAL SOC's USING ANALOG TEST WRAPPERS
Anuja Sehgal (as@ee.duke.edu), Sule Ozev, Krishnendu Chakrabarty - *Duke Univ., Durham, NC*
- 2A.3 USING DISTRIBUTED RECTANGLE BIN PACKING APPROACH FOR CORE-BASED SOC TEST SCHEDULING WITH POWER CONSTRAINT
Yu Xia, Malgorzata E. Chrzanowska-Jeske (jeske@ee.pdx.edu), Benyi Wang - *Portland State Univ., Portland, OR*

Time: 2:00 PM to 3:30 PM

Room: Pine/Fir

SESSION 2B ELECTRICAL AND POWER MODELS - SYSTEM TO TRANSISTOR LEVEL

Moderators: David Overhauser - *Cadence Design Systems, Inc., San Jose, CA*
Farid N. Najm - *Univ. of Toronto, Toronto, ON, Canada*

The three papers in this session cover three levels of abstraction, spanning system level, to block level, to transistor level. The first paper gives models that contribute to power estimation of high-level system descriptions, by propagating moments of the signal pdfs. The second paper is focused on array-based logic, such as memory arrays, and gives power models that factor in technology and architecture parameters. The third paper proposes a fast model for SOI transistors, which can be used in timing and power analysis.

- 2B.1 MOMENT-BASED POWER ESTIMATION IN VERY DEEP SUBMICRON TECHNOLOGIES
Alberto Garcia-Ortiz (agarcia@mes.tu-darmstadt.de), Lukusa Kabulepa, Tudor Murgan, Manfred Glesner - *Technical Univ. of Darmstadt, Darmstadt, Germany*
- 2B.2 IDAP: A TOOL FOR HIGH LEVEL POWER ESTIMATION OF CUSTOM ARRAY STRUCTURES
Mahesh N. Mamidipaka (maheshmn@ics.uci.edu) - *Univ. of California, Irvine, CA*
Kamal Khouri - *Motorola, Inc., Austin, TX*
Nikil Dutt - *Univ. of California, Irvine, CA*
Magdy Abadir - *Motorola, Inc., Austin, TX*
- 2B.3 SOI TRANSISTOR MODEL FOR FAST TRANSIENT SIMULATION
Dmitry Nadezhin - *MCST, Moscow, Russian Federation*
Sergey Gavrilov, **Alexey Glebov**, **Yury Egorov** - *Microstyle, Moscow, Russian Federation*
Vladimir P. Zolotov (vladimir.zolotov@motorola.com) - *Motorola, Inc., Austin, TX*
David Blaauw - *Univ. of Michigan, Ann Arbor, MI*
Rajendran Panda, **Murat Becer**, **Alexandre Ardelea**, **Ajay Patel** - *Motorola, Inc., Austin, TX*

Time: 2:00 PM to 3:30 PM

Room: Donner/Siskiyou

**SESSION 2C • EMBEDDED TUTORIAL: DESIGN AND CAD
CHALLENGES FOR SUB-90NM CMOS TECHNOLOGY**

Moderators: Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*
Thomas Burd - *Consultant, Berkeley, CA*

Scaling the conventional MOSFET beyond the 90nm technology node requires innovations to circumvent barriers due to the fundamental physics that constrains the conventional MOSFET. The limits most often cited are: quantum-mechanical tunneling of carriers through thin gate oxide, from drain to source, and from drain to body; control of the density and location of dopants to provide high I_{on}/I_{off} ratio; and finite subthreshold slope. These fundamental limits have led to the pessimistic predictions of the imminent end of technological progress in semiconductor industry. However, the push to scale conventional MOSFET has continued to show remarkable progress. Continued scaling and demand for performance are pushing for lower supply voltage and V_t , shorter channel length, thinner gate oxide, higher body doping concentration, and thinner Si film thickness. In addition, new materials such as strained-Si channel on relaxed SiGe layer are on the semiconductor roadmap to enhance the mobility and current drive. New device structures such as double-gate FinFETs and 3D circuits are being aggressively pursued for 65nm technology and beyond. Such aggressive scaling and new device structures give rise to several unique design issues which must be dealt with before any of these technologies will gain mainstream acceptance. We will discuss unique design aspects and issues resulting from this scaling such as gate-to-body tunneling, self-heating, reliability issues, and process variations. As the scaling approaches various physical limits, new SOI design issues such as V_t modulation due to leakage, low-voltage impact ionization, and higher V_t , I_{in} to maintain adequate V_t , sat, continue to surface. With an eye towards the future, design and CAD issues related to sub-65nm device structures such as double gate FinFET will be discussed.


PRESENTERS:

Kerry Bernstein - *IBM Corp., Yorktown Heights, NY*
Ching-Te Chuang - *IBM Corp., Yorktown Heights, NY*

CO-AUTHORS:

Rajiv V. Joshi - *IBM Corp., Yorktown Heights, NY*
Ruchir Puri - *IBM Corp., Yorktown Heights, NY*

IT'S NOT TOO LATE....



You can still register for the Full Day Tutorials,
Thursday, November 13, 2003 • 9:00AM - 5:00PM

**Visit the Registration Desk
in the Bayshore Foyer**

Tut 1 - *Linux for EDA*
Tut 2 - *Leakage Issues in IC Design: Trends,
Estimation and Avoidance*
Tut 3 - *Recent Advances in Formal Verification*
Tut 4 - *Embedded Software Development*

see pages 42 - 43 for details

Time: 4:00 PM to 6:00 PM

Room: Cedar

SESSION 3A EMERGING TECHNIQUES IN DYNAMIC VERIFICATION

Moderators: Jay Lawrence - *Cadence Design Systems, Inc., Chelmsford, MA*
Arturo Salz - *Synopsys, Inc., Mountain View, CA*

Challenges created by growing design complexity and size are leading to the development of new techniques in dynamic verification. This session presents how advances in the use of constraint-based stimulus generators, cycle-accurate modeling of pipelines, and monitor circuits are applied to these challenges.

3A.1 FAST CYCLE-ACCURATE BEHAVIORAL SIMULATION FOR PIPELINED PROCESSORS USING EARLY PIPELINE EVALUATION

In-Cheol Park (icpark@ee.kaist.ac.kr), **Sehyeon Kang**, Yongseok Yi - *KAIST, Daejeon, Korea*

3A.2 A FRAMEWORK FOR CONSTRAINED FUNCTIONAL VERIFICATION

Jun Yuan (jy_austin@yahoo.com) - *Cadence Design Systems, Inc., San Jose, CA*
Carl Pixley - *Synopsys, Inc., Hillsboro, OR*
Ken Albin - *Motorola, Inc., Austin, TX*
Adnan Aziz - *Univ. of Texas, Austin, TX*

3A.3 GENERATOR-BASED VERIFICATION

Yunshan Zhu (yunshan@synopsys.com) - *Synopsys, Inc., Mountain View, CA*
James H. Kukula - *Synopsys, Inc., Hillsboro, OR*

3A.4 EFFICIENT GENERATION OF MONITOR CIRCUITS FOR GSTE ASSERTION GRAPHS

Alan J. Hu (ajh@cs.ubc.ca) - *Univ. of British Columbia, Vancouver, BC, Canada*
Jeremy Casas, Jin Yang - *Intel Corp., Hillsboro, OR*

Time: 4:00 PM to 6:00 PM

Room: Pine/Fir

SESSION 3B DELAY AND SIGNAL MODELING FOR TIMING ANALYSIS

Moderators: David J. Hathaway - *IBM Corp., Essex Junction, VT*
Timothy Burks - *Magma Design Automation, Inc., Cupertino, CA*

The session contains a pair of papers describing new signal models and two that detail the effects of power supply variation on delay. The first paper presents a new model for signal transitions based on the Weibull distribution function. The second describes a method for computing an equivalent input waveform that represents a broad range of possible input signals. The next two papers focus on the effects of voltage variation on delay and develop methods for finding the worst-case circuit delay under variations in supply voltage.

3B.1 WEIBULL BASED ANALYTICAL WAVEFORM MODEL

Chirayu S. Amin (c-amin@northwestern.edu) - *Northwestern Univ., Evanston, IL*
Florentin Dartu - *Intel Corp., Hillsboro, OR*
Yehea I. Ismail - *Northwestern Univ., Evanston, IL*

3B.2 EQUIVALENT WAVEFORM PROPAGATION FOR STATIC TIMING ANALYSIS

Masanori Hashimoto (hasimoto@i.kyoto-u.ac.jp), Yuji Yamada, Hidetoshi Onodera - *Kyoto Univ., Kyoto, Japan*

3B.3 TIMING ANALYSIS IN PRESENCE OF POWER SUPPLY AND GROUND VOLTAGE VARIATIONS

Rubil Ahmadi, Farid N. Najm (f.najm@utoronto.ca) - *Univ. of Toronto, Toronto, ON, Canada*

3B.4 VECTORLESS ANALYSIS OF SUPPLY NOISE INDUCED DELAY VARIATION

Sanjay Pant (spant@umich.edu), David Blaauw - *Univ. of Michigan, Ann Arbor, MI*
Savithri Sundareswaran, Vladimir Zolotov, Rajendran Panda - *Motorola Inc., Austin, TX*

Time: 4:00 PM to 6:00 PM

Room: Donner/Siskiyou

SESSION 3C SOFTWARE TECHNIQUES FOR ENERGY AND PERFORMANCE OPTIMIZATION IN EMBEDDED SYSTEMS

Moderator: Grant Martin - *Cadence Design Systems, Inc., Berkeley, CA*

Code transformations have great potential to minimize energy and increase the speed of embedded systems. The papers in this session demonstrate a variety of methods of achieving this. The first paper presents array data transformations for improved memory-access efficiency. The second paper presents a cache-activity minimization technique for real-time embedded systems. The third paper combines compression and functional partitioning techniques for energy optimization. The last paper combines fault tolerance with the other concerns of energy optimizations systems.

3C.1 ARRAY COMPOSITION AND DECOMPOSITION FOR OPTIMIZING EMBEDDED APPLICATIONS

Guilin Chen, Mahmut Kandemir (mtkandemir@hotmail.com) - *Penn State Univ., State College, PA*
 Ugur Sezer - *Univ. of Wisconsin, Madison, WI*
 Avanti Nadgir - *Penn State Univ., State College, PA*

3C.2 CODE PLACEMENT WITH SELECTIVE CACHE ACTIVITY MINIMIZATION FOR EMBEDDED REAL-TIME SOFTWARE DESIGN

Junhyung Um - *Samsung Electronics, Suwon, Korea*
 Taewhan Kim (tkim@cs.kaist.ac.kr) - *KAIST, Daejeon, Korea*

3C.3 ENERGY OPTIMIZATION OF DISTRIBUTED EMBEDDED PROCESSORS BY COMBINED DATA COMPRESSION AND FUNCTIONAL PARTITIONING

Jinfeng Liu (jinfengl@ece.uci.edu), Pai H. Chou - *Univ. of California, Irvine, CA*

3C.4 ENERGY-AWARE FAULT TOLERANCE IN FIXED-PRIORITY REAL-TIME EMBEDDED SYSTEMS

Ying Zhang (yingzh@ee.duke.edu), Krishnendu Chakrabarty, Vishnu Swaminathan - *Duke Univ., Durham, NC*

Time: 4:00 PM to 6:00 PM

Room: Oak

SESSION 3D OPTIMIZATION OF GLOBAL INTERCONNECTS

Moderators: Martin D.F. Wong - *Univ. of Illinois, Urbana, IL*

Atsushi Takahashi - *Tokyo Institute of Tech., Tokyo, Japan*

In this session, three techniques for overcoming the bottleneck introduced by global interconnects are considered: pipelined global interconnects, latency insensitive communication channels, and clock scheduling. The first two papers address the problem of retiming with consideration of pipelined global interconnects. The third paper considers sizing of buffer queues of global communication channels in latency insensitive systems. The fourth paper presents a new method for clock scheduling and clock tree construction that improves the performance of high-end ASICs.

3D.1 RETIMING FOR WIRE PIPELINING IN SYSTEM-ON-CHIP

Chuan Lin (clin@ece.nwu.edu), Hai Zhou - *Northwestern Univ., Evanston, IL*

3D.2 RETIMING WITH INTERCONNECT AND GATE DELAY

Chris Chu (cnchu@iastate.edu) - *Iowa State Univ., Ames, IA*
 Evangeline F.Y. Young, Dennis K.Y. Tong - *The Chinese Univ. of Hong Kong, New Territories, Hong Kong*
 Sampath Dechu - *Iowa State Univ., Ames, IA*

3D.3 PERFORMANCE OPTIMIZATION OF LATENCY INSENSITIVE SYSTEMS THROUGH BUFFER QUEUE SIZING

Ruibing Lu (lur@ecn.purdue.edu), Cheng-Kok Koh - *Purdue Univ., West Lafayette, IN*

3D.4 CLOCK SCHEDULING AND CLOCK TREE CONSTRUCTION FOR HIGH PERFORMANCE ASICS

Stephan Held (held@or.uni-bonn.de), Bernhard Korte, Jens Mafberg - *Univ. of Bonn, Bonn, Germany*
 Matthias Ringe - *IBM Corp., Bonn, Germany*
 Jens Vygen - *Univ. of Bonn, Bonn, Germany*

Time: 8:30 AM to 10:00 AM

Room: Cedar

SESSION 4A NUMERICAL METHODS FOR ANALOG OPTIMIZATION AND ANALYSIS

Moderators: Eric Bracken - *Ansoft Corp., Pittsburgh, PA*
Joel R. Phillips - *Cadence Berkeley Labs., San Jose, CA*

This session introduces a variety of new numerical methods for the automated design and analysis of analog circuits. The first paper contributes to more efficient analog circuit optimization by helping the optimizer to find the center of the feasible design parameter space. The second discusses methods for calculating phase noise in oscillators. The final paper in the session describes an improved time-domain preconditioner for solving the harmonic balance equations.

4A.1 INITIAL SIZING OF ANALOG INTEGRATED CIRCUITS BY CENTERING WITHIN TOPOLOGY-GIVEN IMPLICIT SPECIFICATIONS

Guido Stehr (guido.stehr@eda.ei.tum.de) - *Technical Univ. of Munich, Munich, Germany*
Michael Pronath, Frank Schenkel - *MunEDA GmbH, Riemerling, Germany*
Helmut Graeb, Kurt Antreich - *Technical Univ. of Munich, Munich, Germany*

4A.2 A GENERALIZED METHOD FOR COMPUTING OSCILLATOR PHASE NOISE SPECTRA

Piet Vanassche (piet.vanassche@esat.kuleuven.ac.be) - *ESAT/Micas, Leuven, Belgium*
Georges G. Gielen, Willy Sansen - *Katholieke Univ., Leuven, Belgium*

4A.3 EFFICIENT ITERATIVE TIME PRECONDITIONERS FOR HARMONIC BALANCE RF CIRCUIT SIMULATION

Fabrice Veerse (Fabrice_Veerse@mentor.com) - *Mentor Graphics (Ireland) Ltd., Saint Ismier, France*

Time: 8:30 AM to 10:00 AM

Room: Pine/Fir

SESSION 4B CAD ALGORITHMS FOR EMERGING TECHNOLOGIES

Moderators: Bernard Courtois - *TIMA Labs., Grenoble, France*
Michael R. Butts - *Cadence Design Systems, Inc., Portland, OR*

This session focuses on the application of classical CAD algorithms to emerging technology. The first paper considers the application of synthesis to reversible logic. The second paper applies VLSI CAD placement techniques for the design of DNA probe array chips. The third paper applies numerical simulation and reduced order modeling techniques for the dynamic analysis of MEMS.

4B.1 FREDKIN/TOFFOLI TEMPLATES FOR REVERSIBLE LOGIC SYNTHESIS

Dmitri Maslov - *Univ. of New Brunswick, Fredericton, NB, Canada*
Gerhard W. Dueck (mmiller@csr.uvic.ca), David M. Miller - *Univ. of Victoria, Victoria, BC, Canada*

4B.2 EVALUATION OF PLACEMENT TECHNIQUES FOR DNA PROBE ARRAY LAYOUT

Sherief Reda (sreda@cs.ucsd.edu), Andrew B. Kahng, Ion Mandoiu, Xu Xu - *Univ. of California at San Diego, La Jolla, CA*
Alex Zelikovskiy - *Georgia State Univ., Atlanta, GA*

4B.3 PHYSICAL AND REDUCED-ORDER DYNAMIC ANALYSIS OF MEMS

Sudipto Kumar DE, Narayan Aluru (aluru@uiuc.edu) - *Univ. of Illinois, Urbana, IL*

Time: 8:30 AM to 10:00 AM

Room: Donner/Siskiyou

SESSION 4C DESIGN TECHNIQUES FOR CUSTOMIZED PROCESSORS

Moderators: Radu Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*
 Tony Givargis - *Univ. of California, Irvine, CA*

This session deals with the design of application specific processors. The papers cover a wide spectrum of issues ranging from instruction selection to processor synthesis and DSP specific arithmetic design issues.

4C.1 FAST, ACCURATE STATIC ANALYSIS FOR FIXED-POINT FINITE PRECISION EFFECTS IN DSP DESIGNS

Claire F. Fang (ffang@cmu.edu), Rob A. Rutenbar, Tsuhan Chen - *Carnegie Mellon Univ., Pittsburgh, PA*

4C.2 A SCALABLE APPLICATION-SPECIFIC PROCESSOR SYNTHESIS METHODOLOGY

Fei Sun (fsun@princeton.edu) - *Princeton Univ., Princeton, NJ*
 Srivaths Ravi, Anand Raghunathan - *NEC Labs., Princeton, NJ*
 Niraj K. Jha - *Princeton Univ., Princeton, NJ*

4C.3 INSIDE: INSTRUCTION SELECTION/IDENTIFICATION & DESIGN EXPLORATION FOR EXTENSIBLE PROCESSOR

Newton Cheung (ncheung@cse.unsw.edu.au) - *Univ. of New South Wales, Sydney, Australia*
 Joerg Henkel - *NEC Labs., Princeton, NJ*
 Sri Parameswaran - *Univ. of New South Wales, Sydney, Australia*

Time: 8:30 AM to 10:00 AM

Room: Oak

SESSION 4D NEW IMPROVEMENTS IN PLACEMENT

Moderators: Kia Bazargan - *Univ. of Minnesota, Minneapolis, MN*
 Salil Rajc - *Hier Design, Inc., Santa Clara, CA*

This session presents novel ideas that significantly improve the performance of existing placement methods. The first paper decreases wirelength of mPL1. The second paper revises the standard mincut partitioning framework and proposes a new dynamic programming algorithm for legalization. The third paper improves Capo on regular circuits, discusses better whitespace allocation and evaluates a method to stabilize successive placement iterations.

4D.1 AN ENHANCED MULTILEVEL ALGORITHM FOR CIRCUIT PLACEMENT

Tony F. Chan, Jason Cong - *Univ. of California, Los Angeles, CA*
 Tim Kong - *Magma Design Automation, Inc., Los Angeles, CA*
 Joseph R. Shinnerl (shinnerl@cs.ucla.edu), **Kenton Sze** - *Univ. of California, Los Angeles, CA*

4D.2 FRACTIONAL CUT: IMPROVED RECURSIVE BISECTION PLACEMENT

Ameya Agnihotri, Mehmet C. Yildiz, Ateen Khatkhate, Ajita Mathur, Satoshi Ono, **Patrick H. Madden** (pmadden@cs.binghamton.edu) - *State Univ. of New York, Binghamton, NY*

4D.3 ON WHITESPACE AND STABILITY IN MIXED-SIZE PLACEMENT AND PHYSICAL SYNTHESIS

Saurabh N. Adya, Igor L. Markov (imarkov@eecs.umich.edu) - *Univ. of Michigan, Ann Arbor, MI*
 Paul G. Villarrubia - *IBM Corp., Austin, TX*

Time: 10:30 AM to 12:00 PM

Room: Cedar

SESSION 5A OPTIMIZATIONS FOR VERIFICATION ENGINES

Moderators: Aarti Gupta - *NEC Labs., Princeton, NJ*
Eugene Goldberg - *Cadence Berkeley Labs., Berkeley, CA*

The papers in this session explore how different combinations of techniques from automatic test pattern generation (ATPG), Boolean satisfiability (SAT), and Binary Decision Diagrams (BDDs) can be combined to improve the core algorithms in various formal verification applications. The optimizations include exploiting time frame expansions, multi-valued encodings, and over-approximations of reachable states.

5A.1 SATORI – A FAST SEQUENTIAL SAT ENGINE FOR CIRCUITS

Madhu Iyer, Ganapathy Parthasarathy
(gpartha@windcave.ece.ucsb.edu), Kwang-Ting (Tim) Cheng -
Univ. of California, Santa Barbara, CA

5A.2 CAMA: A MULTI-VALUED SATISFIABILITY SOLVER

Cong Liu - *Univ. of California, Berkeley, CA*
Andreas Kuehlmann - *Cadence Berkeley Labs., Berkeley, CA*
Matthew W. Moskewicz - *Univ. of California, Berkeley, CA*

5A.3 THE COMPOSITIONAL FAR SIDE OF IMAGE COMPUTATION

Chao Wang (wangc@colorado.edu), Gary D. Hachtel, Fabio
Somenzi - *Univ. of Colorado, Boulder, CO*

SESSION 5B SYSTEM DESIGN CONCEPTS

Moderators: N. Vijaykrishnan - *Penn State Univ., University Park, PA*
Yatin Hoskote - *Intel Corp., Portland, OR*

Three concepts are presented for various aspects of system design. The first presents an analytical approach to substantially speed-up the modeling of cache performance. The second presents a novel method of process migration to improve the fault tolerance of distributed systems. The third demonstrates a new programming model to improve the performance of system-on-chip platforms.

5B.1 CACHE OPTIMIZATION FOR EMBEDDED PROCESSOR CORES: AN ANALYTICAL APPROACH

Arijit Ghosh (arijitg@ics.uci.edu), Tony Givargis - *Univ. of
California, Irvine, CA*

5B.2 FAULT-TOLERANT TECHNIQUES FOR AMBIENT INTELLIGENT DISTRIBUTED SYSTEMS

Diana Marculescu (dianam@ece.cmu.edu), Nicholas H.
Zamora, Phillip Stanley-Marbell, Radu Marculescu - *Carnegie
Mellon Univ., Pittsburgh, PA*

5B.3 PERFORMANCE EFFICIENCY OF CONTEXT-FLOW SYSTEM-ON-CHIP PLATFORM

Rami Beidas (rbeidas@eecg.toronto.edu), Jianwen Zhu - *Univ.
of Toronto, Toronto, ON, Canada*

Time: 10:30 AM to 12:00 PM

Room: Pine/Fir

Time: 10:30 AM to 12:30 PM

Room: Donner/Siskiyou

SESSION 5C ANALOG DESIGN AND METHODOLOGY

Moderators: Kenneth Kundert - *Cadence Design Systems, Inc., San Jose, CA*
 Georges G. Gielen - *Katholieke Univ., Leuven, Belgium*

This session includes four papers that focus on the design of analog circuits. The first formulates a new definition for noise figure in the context of multistage ultrawideband communication systems. The next two address pipelined ADCs. The first derives formulas that predict the distortion that results from gain and capacitive mismatch errors. The second considers the most common design variations and derives formulas that relate expected performance metrics to the various design parameters. The final paper proposes the concept of analog measurements and assertions as a way of supporting both the initial design process and reuse.

5C.1 AMPLIFICATION OF ULTRAWIDEBAND SIGNALS

Won Namgoong (namgoong@usc.edu), Jongrit Lerdworatawee - *Univ. of Southern California, Los Angeles, CA*

5C.2 A STATISTICAL APPROACH TO ESTIMATE THE DYNAMIC NON-LINEARITY PARAMETERS OF PIPELINE ADCs

Mohammad Taherzadeh-Sani (taherzadeh_m@yahoo.com), Reza Lotfi, **Omid Shoaee** - *Univ. of Tehran, Tehran, Iran*

5C.3 SYSTEMATIC DESIGN FOR POWER MINIMIZATION OF PIPELINED ANALOG-TO-DIGITAL CONVERTERS

Reza Lotfi (lotfireza@yahoo.com), Mohammad Taherzadeh-Sani, Mohammad Yaser Azizi, **Omid Shoaee** - *Univ. of Tehran, Tehran, Iran*

5C.4 A FRAMEWORK FOR DESIGNING RELISABLE ANALOG CIRCUITS

Dean T. Liu (dliu@stanford.edu) - *Stanford Univ., Stanford, CA*
 Stefanos Sidiropoulos - *Aeluros Inc., Mountain View, CA*
 Mark Horowitz - *Stanford Univ., Stanford, CA*

Time: 10:30 AM to 12:30 PM

Room: Oak

SESSION 5D ROUTING

Moderators: Hai Zhou - *Northwestern Univ., Evanston, IL*
 Charles Chiang - *Synopsys, Inc., Mountain View, CA*

Routing continues to be a challenging problem. In this session, we present new techniques for routing. The first paper presents a multi-level routing system that considers crosstalk and performance. The second paper presents a detailed router for FPGAs based on network flow computation. The third paper presents length-matching techniques for routing high-speed PCB boards. Finally, the fourth paper gives an upper bound for clock skew due to wire width variation.

5D.1 A FAST CROSSTALK- AND PERFORMANCE-DRIVEN MULTILEVEL ROUTING SYSTEM

Tsung Yi Ho, Yao Wen Chang (ywchang@cc.ee.ntu.edu.tw), Sao Jie Chen - *National Taiwan Univ., Taipei, Taiwan*
 D. T. Lee - *IIS Sinica, Taipei, Taiwan*

5D.2 A MIN-COST FLOW BASED DETAILED ROUTER FOR FPGAs

Seokjin Lee (seokjin@cs.utexas.edu), Yongseok Cheon - *Univ. of Texas, Austin, TX*
 Martin D.F. Wong - *Univ. of Illinois, Urbana, IL*

5D.3 LENGTH-MATCHING ROUTING FOR HIGH-SPEED PRINTED CIRCUIT BOARDS

Muhammet M. Ozdal (ozdal@uiuc.edu), Martin D.F. Wong - *Univ. of Illinois, Urbana, IL*

5D.4 ANALYTICAL BOUND FOR UNWANTED CLOCK SKEW DUE TO WIRE WIDTH VARIATION

Anand K. Rajaram - *Texas A&M, College Station, TX*
 Wei Guo - *Institut Francais du P trole, Rueil-Malmaison, France*
 Bing Lu - *Cadence Design Systems, Inc., New Providence, NJ*
 Rabi N. Mahapatra, Jiang Hu (jianghu@ee.tamu.edu) - *Texas A&M, College Station, TX*

Time: 2:00 PM to 3:30 PM

Room: Cedar

SESSION 6A AUTOMATIC ABSTRACTION FOR FORMAL VERIFICATION

Moderators: James H. Kukula - *Synopsys, Inc., Hillsboro, OR*
Ken McMillan - *Cadence Berkeley Labs., Berkeley, CA*

State space explosion sets severe limitations on exact formal analysis. Abstraction is a key to reducing state explosion, enabling the verification of industrial designs. This session presents two new methods of incremental abstraction based on SAT, and a novel technique of timing abstraction that allows efficient verification of timed asynchronous circuits.

6A.1 IMPROVING ARIADNE'S BUNDLE BY FOLLOWING MULTIPLE THREADS IN ABSTRACTION REFINEMENT

Chao Wang (wangc@colorado.edu), Bing Li, HoonSang Jin, Gary D. Hachtel, Fabio Somenzi - *Univ. of Colorado, Boulder, CO*

6A.2 ITERATIVE ABSTRACTION USING SAT-BASED BMC WITH PROOF ANALYSIS

Aarti Gupta (agupta@nec-labs.com), Malay Ganai, Pranav Ashar, Zijiang Yang - *NEC Labs., Princeton, NJ*

6A.3 EFFICIENT VERIFICATION OF HAZARD-FREEDOM IN GATE-LEVEL TIMED ASYNCHRONOUS CIRCUITS

Curtis A. Nelson, Chris J. Myers (myers@vlsigroup.ece.utah.edu) - *Univ. of Utah, Salt Lake City, UT*
Tomohiro Yoneda - *Tokyo Institute of Tech., Tokyo, Japan*

Time: 2:00 PM to 3:30 PM

Room: Pine/Fir

SESSION 6B EMBEDDED TUTORIAL: SYSTEM LEVEL DESIGN AND VERIFICATION USING A SYNCHRONOUS LANGUAGE

Moderators: Nikil Dutt - *Univ. of California, Irvine, CA*
Joerg Henkel - *NEC Labs., Princeton, NJ*

Synchronous languages (Esterel, Lustre, and others) have been invented for formal specification and embedded software compilation in safety critical applications. Recent advances in Esterel further extended the scope of applications to RTL compilation. Contrary to traditional HDL languages (Verilog, VHDL) and recent system-level languages (SystemC, System Verilog) synchronous languages have well defined formal semantics which facilitates bug avoidance using correct-by-construction compilation and verification. This tutorial will demonstrate what synchronous languages have to offer for the modeling, design, analysis and implementation of systems that comprise hardware and software. The requirement for a system notation that spans hardware and software and which also facilitates combined hardware/software static analyses has become especially acute now that vendors produce devices that contain configurable logic and embedded microprocessors. Case studies will include examples of design space exploration by synthesizing hardware or software from the same description; static analysis of system level properties e.g. maximum latency on communication channels and formal verification of safety properties (e.g. bus protocol conformance). We shall also show how the output of this synchronous system level design methodology can be used in conjunction with other system level tools and how one can use a synchronous approach to model IP blocks at a high level of abstraction. Such models have proved to be useful for rapid design space exploration and verification at a system level without requiring detailed implementation and slow bit-level event-based simulation. We will also address some of the issues of RTL compilation (code controllability, ECO, optimization) difficult in high-level design flows. We conclude with the review of research directions.

PRESENTERS:

Gerard Berry - *Esterel Technologies, Villeneuve, Loubert, France*
Mike Kishinevsky - *Intel Corp., Hillsboro, OR*
Satnam Singh - *Xilinx, Inc., San Jose, CA*

Time: 2:00 PM to 3:30 PM

Room: Donner/Siskiyou

SESSION 6C NONLINEAR MODELLING OF ANALOG AND OPTICAL SYSTEMS

Moderators: Jaijeet Roychowdhury - *Univ. of Minnesota, Minneapolis, MN*
 Mustafa Celik - *Magma Design Automation, Inc., Cupertino, CA*

This session presents recent advances in the modelling and compaction of nonlinear analog and continuous systems. The first paper presents a number of novel advances and computational techniques for non-Monte-Carlo noise analysis of long-haul optical fiber systems. The second paper introduces new and efficient techniques for nonlinear model reduction based on Kernel methods. The third paper presents a method for efficient nonlinear macromodel generation via accelerated pruning of higher-order system matrices.

6C.1 NOISE ANALYSIS FOR OPTICAL FIBER COMMUNICATION SYSTEMS

Alper Demir (aldemir@ku.edu.tr) - *KOC Univ., Sariyer-Istanbul, Turkey*

6C.2 ANALOG MACROMODELING USING KERNEL METHODS

Joel R. Phillips (jrp@cadence.com) - *Cadence Berkeley Labs., San Jose, CA*
 Joao Pedro Afonso, Arlindo Oliveira, Miguel Silveira - *INESC/Technical Univ. Lisbon, Lisbon, Portugal*

6C.3 A HYBRID APPROACH TO NONLINEAR MACROMODEL GENERATION FOR TIME-VARYING ANALOG CIRCUITS

Peng Li (pli@ece.cmu.edu), Xin Li, Yang Xu, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

Time: 2:00 PM to 3:30 PM

Room: Oak

SESSION 6D TIMING AND TRADEOFFS IN PLACEMENT

Moderators: Igor L. Markov - *Univ. of Michigan, Ann Arbor, MI*
 Rajeev Jayaraman - *Xilinx, Inc., San Jose, CA*

Successful circuit layout often requires trade-offs, especially when timing optimization affects other design objectives. The first paper proposes an incremental optimization of circuit delay while keeping wirelength low. The second paper trades off runtime and the strength of optimization to improve the results of wirelength-driven placement. The third paper studies the quality and stability of timing-driven placement algorithms.

6D.1 INCREMENTAL PLACEMENT FOR TIMING OPTIMIZATION

Wonjoon Choi (wjchoi@ece.umn.edu), Kia Bazargan - *Univ. of Minnesota, Minneapolis, MN*

6D.2 A TRADEOFF-ORIENTED PLACEMENT TOOL

Huaiyu Xu (huaiyu@cs.ucla.edu), Bo-Kyung Choi, Majid Sarrafzadeh - *Univ. of California, Los Angeles, CA*

6D.3 OPTIMALITY AND STABILITY STUDY OF TIMING-DRIVEN PLACEMENT ALGORITHMS

Jason Cong, **Michail Romesis** (michail@cs.ucla.edu), Min Xie - *Univ. of California, Los Angeles, CA*

Time: 4:00 PM to 6:00 PM

Room: Cedar

SESSION 7A SIMULATION AT THE NANOMETER SCALE

Moderators: Kenneth Kundert - *Cadence Design Systems, Inc., San Jose, CA*
Narayan Aluru - *Univ. of Illinois, Urbana, IL*

Nanoscale technologies demand new CAD techniques. This session explores approaches to modeling and simulation of nanoscale technologies and systems. The first paper uses the model of a Markov Random Network for fault-tolerant computing. The following three papers all present circuit simulation methods for carbon nanotubes (CNTs), resonant tunneling diodes (RTDs), and, single-electron transistors (SETs) mixed with CMOS.

7A.1 A PROBABILISTIC-BASED DESIGN METHODOLOGY
FOR NANO-SCALE COMPUTATION

Joseph Mundy, Jie Chen, **Iris Bahar** (iris_bahar@brown.edu) -
Brown Univ., Providence, RI

7A.2 MODELING OF BALLISTIC CARBON NANOTUBE FIELD EFFECT
TRANSISTORS FOR EFFICIENT CIRCUIT SIMULATION

Arijit Raychowdhury (araycho@ecn.purdue.edu), Saibal
Mukhopadhyay, Kaushik Roy - *Purdue Univ., West Lafayette, IN*

7A.3 CIRCUIT SIMULATION OF NANOTECHNOLOGY DEVICES WITH NON-
MONOTONIC I-V CHARACTERISTICS

Jiayong Le (jiayongl@ece.cmu.edu), Lawrence Pileggi - *Carnegie
Mellon Univ., Pittsburgh, PA*
Anirudh Devgan - *IBM Corp., Austin, TX*

7A.4 A CAD FRAMEWORK FOR CO-DESIGN AND ANALYSIS
OF CMOS-SET HYBRID INTEGRATED CIRCUITS

Santanu Mahapatra - *Swiss Federal Institute of Tech.,
Lausanne, Switzerland*
Kaustav Banerjee - *Univ. of California, Santa Barbara, CA*
Florent Pegeon - *Silvaco Data Systems, Grenoble, France*
Adrian M. Ionescu (Adrian.Ionescu@epfl.ch) - *Swiss Federal
Institute of Tech., Lausanne, Switzerland*

SESSION 7B ENERGY ISSUES IN SYSTEMS DESIGN

Moderators: Wolfgang Nebel - *Oldenburg Univ. and OFFIS Research
Intitute, Oldenburg, Germany*
Marcello Lajolo - *NEC Labs., Princeton, NJ*

This session provides a broad coverage of techniques in system level energy optimization, ranging from high level approaches building on dynamic adaptation of modulation in transceivers and task level scheduling with voltage selection to novel techniques for cache replacement policy and register renaming algorithms.

7B.1 A GAME THEORETIC APPROACH TO DYNAMIC ENERGY MINIMIZATION
IN WIRELESS TRANSCEIVERS

Ali Iranli, Hanif E. Fatemi (fatemi@usc.edu), Massoud Pedram -
Univ. of Southern California, Los Angeles, CA

7B.2 COMMUNICATION-AWARE TASK SCHEDULING AND VOLTAGE
SELECTION FOR TOTAL SYSTEMS ENERGY MINIMIZATION

Girish V. Varatkar, **Radu Marculescu** (radum@ece.cmu.edu) -
Carnegie Mellon Univ., Pittsburgh, PA

7B.3 LRU-SEQ: A NOVEL REPLACEMENT POLICY FOR TRANSITION ENERGY
REDUCTION IN INSTRUCTION CACHES

Praveen G. Kalla (nkalla@cse.nd.edu), Xiaobo (Sharon) Hu - *Univ.
of Notre Dame, Notre Dame, IN*
Joerg Henkel - *NEC Labs., Princeton, NJ*

7B.4 COMPILER-BASED REGISTER NAME ADJUSTMENT
FOR LOW-POWER EMBEDDED PROCESSORS

Alex Orailoglu - *Univ. of California at San Diego, La Jolla, CA*

19 Time: 4:00 PM to 6:00 PM

Room: Pine/Fir

Time: 4:00 PM to 6:00 PM

Room: Donner/Siskiyou

**SESSION 7C CONSTRAINT DRIVEN
HIGH-LEVEL SYNTHESIS**

Moderators: Michael Kishinevsky - *Intel Corp., Hillsboro, OR*
Barry Pangrle - *Synopsys, Inc., Mountain View, CA*

The quality of high-level synthesis is improved by integration with physical placement, interconnect modeling, and minimal commitment heuristics. The first paper describes general principles for development of effective heuristics. The next two papers integrate placement and HLS techniques. The final paper describes high level power estimation for global interconnect.

**7C.1 GRADUAL RELAXATION TECHNIQUES
FOR SYSTEM SYNTHESIS**

Zhiru Zhang, **Yiping Fan** (fanyp@cs.ucla.edu), Miodrag Potkonjak, Jason Cong - *Univ. of California, Los Angeles, CA*

**7C.2 ARCHITECTURAL SYNTHESIS INTEGRATED WITH GLOBAL
PLACEMENT FOR MULTI-CYCLE COMMUNICATION**

Jason Cong, Yiping Fan, Guoling Han, Xun Yang, **Zhiru Zhang** (zhiruz@cs.ucla.edu) - *Univ. of California, Los Angeles, CA*

**7C.3 BINDING, ALLOCATION AND FLOORPLANNING
IN LOW POWER HIGH-LEVEL SYNTHESIS**

Ansgar Stammermann (ansgar.stammermann@offis.de), Domenik Helms, Milan Schulte - *OFFIS Research Institute, Oldenburg, Germany*
Arne Schulz - *Univ. of Oldenburg, Oldenburg, Germany*
Wolfgang Nebel - *OFFIS Research Institute & Univ. of Oldenburg, Oldenburg, Germany;*

**7C.4 A HIGH-LEVEL INTERCONNECT POWER
MODEL FOR DESIGN SPACE EXPLORATION**

Pallav Gupta (pallav@ieee.org), Lin Zhong, Niraj K. Jha - *Princeton Univ., Princeton, NJ*

Time: 4:00 PM to 6:00 PM

Room: Oak

**SESSION 7D OPTIMAL INTERCONNECT SYNTHESIS AND
ANALYSIS**

Moderators: Leon Stok - *IBM Corp., Yorktown Heights, NY*
John P. Fishburn - *Consultant, Murray Hill, NJ*

Technology projections show that an increasing percentage of chip power and delay is going to interconnections. The papers in this session present new insights in how to minimize the classic cost metrics of power, delay and area, while adding new considerations of delay variability and latency.

7D.1 A PROBABILISTIC APPROACH TO BUFFER INSERTION

Vishal Khandelwal (vishalk@glue.umd.edu), Azadeh Davoodi - *Univ. of Maryland, College Park, MD*
Akash Nanavati - *Univ. of California, Los Angeles, CA*
Ankur Srivastava - *Univ. of Maryland, College Park, MD*

**7D.2 SIMULTANEOUS ANALYTIC AREA AND POWER OPTIMIZATION FOR
REPEATER INSERTION**

Giuseppe Garcea (g.garcea@its.tudelft.nl), Nick P. van der Meijs - *Delft Univ. of Tech., Delft, The Netherlands*
Ralph H.J.M. Otten - *Eindhoven Univ. of Tech., Eindhoven, The Netherlands*

**7D.3 FULL-CHIP INTERCONNECT POWER ESTIMATION
AND SIMULATION CONSIDERING CONCURRENT REPEATER AND
FLIP-FLOP INSERTION**

Weiping Liao (wliao@ee.ucla.edu), Lei He - *Univ. of California, Los Angeles, CA*

**7D.4 POWER-OPTIMAL SIMULTANEOUS BUFFER INSERTION/SIZING AND
WIRE SIZING**

Ruiming Li (rl18@utdallas.edu), Dian Zhou, Jin Liu - *Univ. of Texas at Dallas, Richardson, TX*
Xuan Zeng - *Fudan Univ., Shanghai, China*

Time: 8:30 AM to 10:00 AM

Room: Cedar

SESSION 8A MEMORY TESTING

Moderators: Yervant Zorian - *Virage Logic Corp., Fremont, CA*
Adit Singh - *Auburn Univ., Montgomery, AL*

The push of technology frontiers by large memories results in increased incidence of errors. Correcting such errors through innovative BISR is explored in the first paper. The second paper provides a failure analysis framework for identifying the fault location. The large sizes of memories and the systems within which they are embedded necessitates attention to hardware/software co-testing of embedded memories, as explored in the final paper.

8A.1 DYNAMIC DATA-BIT MEMORY BUILT-IN SELF-REPAIR

Michael Nicolaidis (michael.nicolaidis@iroctech.com), Nadir Achouri, Slimane Boutobza - *iRoC Tech., Grenoble, France*

8A.2 FAME: A FAULT-PATTERN BASED MEMORY FAILURE ANALYSIS FRAMEWORK

Kuo Liang Cheng, Chih Wea Wang, Jih Nung Lee, Yung Fa Chou, **Chih-Tsun Huang** (cthuan@larc.ee.nthu.edu.tw), Cheng Wen Wu - *National Tsing-Hua Univ., Hsinchu, Taiwan*

8A.3 HARDWARE/SOFTWARE CO-TESTING OF EMBEDDED MEMORIES IN COMPLEX SOCS

Bai Hong Fang, Qiang Xu, Nicola Nicolici (nicola@ece.mcmaster.ca) - *McMaster Univ., Hamilton, ON, Canada*

Time: 8:30 AM to 10:00 AM

Room: Pine/Fir

SESSION 8B STATISTICAL STATIC TIMING - I

Moderators: Louis Scheffer - *Cadence Design Systems, Inc., San Jose, CA*
Duncan M. (Hank) Walker - *Texas A&M Univ., College Station, TX*

Manufacturing induced timing variability has been recognized as one for the top new challenges of the DSM era. The papers in this session deal with the emerging area of statistical static timing analysis, a technique that holds promise in enabling the efficient incorporation of the impact of physical and environmental variability on overall design performance. This is an exciting emerging research area that will be the eventual interface between the integrated circuit manufacturing community and the timing signoff process.

8B.1 BLOCK-BASED STATIC TIMING ANALYSIS WITH UNCERTAINTY

Anirudh Devgan (devgan@us.ibm.com), Chandramouli Kashyap - *IBM Corp., Austin, TX*

8B.2 TAU: TIMING ANALYSIS UNDER UNCERTAINTY

Sarvesh Bhardwaj (sarvesh@ece.arizona.edu), Sarma B. Vrudhula - *Univ. of Arizona, Tucson, AZ*
David Blaauw - *Univ. of Michigan, Ann Arbor, MI*

8B.3 STATISTICAL TIMING ANALYSIS CONSIDERING SPATIAL CORRELATIONS USING A SINGLE PERT-LIKE TRAVERSAL

Hongliang Chang (hchang@cs.umn.edu), Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

Time: 8:30 AM to 10:00 AM

Room: Donner/Siskiyou

SESSION 8C POWER-AWARE DESIGN

Moderators: Tanay Karnik - *Intel Corp., Hillsboro, OR*
 Borivoje Nikolic - *Univ. of California, Berkeley, CA*

Three different concepts in power-aware design are presented. The first minimizes leakage power by optimizing threshold voltages in multi-level caches. The second presents energy-conscious metrics for fault-tolerant battery-operated systems. The third couples dynamic energy-performance scaling with dynamic sub-system reconfigurability for system-on-chip.

8C.1 LEAKAGE POWER OPTIMIZATION TECHNIQUES FOR ULTRA DEEP SUB-MICRON MULTI-LEVEL CACHES

Nam Sung Kim (kimns@eecs.umich.edu), David Blaauw, Trevor N. Mudge - *Univ. of Michigan, Ann Arbor, MI*

8C.2 DYNAMIC FAULT-TOLERANCE AND METRICS FOR BATTERY POWERED, FAILURE-PRONE SYSTEMS

Phillip Stanley-Marbell (pstanley@ece.cmu.edu), Diana Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*

8C.3 DYNAMIC PLATFORM MANAGEMENT FOR CONFIGURABLE PLATFORM-BASED SYSTEM-ON-CHIPS

Krishna Sekar (ksekar@ece.ucsd.edu), Kanishka Lahiri, Sujit Dey - *Univ. of California at San Diego, La Jolla, CA*

Time: 8:30 AM to 10:00 AM

Room: Oak

SESSION 8D INTERCONNECT REDUCTION

Moderators: Chung-Kuan Cheng - *Univ. of California at San Diego, La Jolla, CA*
 Eli Chiprout - *Intel Corp., Chandler, AZ*

This session covers circuit reduction of large interconnect networks. The first paper adopts a hierarchical approach to extract the transfer function. The approach is generalized to arbitrary linear circuits. The second paper provides guided operations to merge branches and eliminate nodes. The third paper proposes a statistical process to extract moments with efficiency.

8D.1 A GENERAL s-DOMAIN HIERARCHICAL NETWORK REDUCTION ALGORITHM

Sheldon X.-D. Tan (stan@ee.ucr.edu) - *Univ. of California, Riverside, CA*

8D.2 BRANCH-MERGE REDUCTION OF RLCM NETWORKS

Bernard N. Sheehan (bernie_sheehan@mentorg.com) - *Mentor Graphics Corp., Wilsonville, OR*

8D.3 A SUM-OVER-PATHS IMPULSE-RESPONSE MOMENT-EXTRACTION ALGORITHM FOR IC-INTERCONNECT NETWORKS: VERIFICATION, COUPLED RC LINES

Yannick L. Le Coz (lecozy@rpi.edu), **Dhivya Krishna** - *Rensselaer Polytechnic Institute, Troy, NY*
 Dusan M. Petranovic, William M. Loh, Peter Bendix - *LSI Logic Corp., Milpitas, CA*

Time: 10:30 AM to 12:00 PM

Room: Cedar

SESSION 9A EMBEDDED TUTORIAL: MIXED SIGNAL DFT: A CONCISE OVERVIEW

Moderators: Erik Larsson - *Link ping Univ., Link ping, Sweden*
Sule Ozev - *Duke Univ., Durham, NC*

This embedded tutorial presents a general overview of current mixed-signal DFT techniques and practices. It starts with a brief summary of basic differences and similarities between mixed signal test and other tests such as digital, memories, and RF. The justifications of functional versus structural fault coverage are discussed. Practical mixed-signal DFT solutions are presented with an accent on performance, cost, and test coverage. Special consideration is dedicated to the recent developments in mixed-signal DFT within a System-On-a-Chip (SoC) environment. A detailed and critical overview of possible DFT techniques for Phase-Locked Loops (PLLs) is provided with associated implications on test coverage, performance, cost, and time to market. A practical PLL case study shows the detailed technical solution with the analysis of possible implementations and related economics. An introduction to DFT techniques for data converters (A/D and D/A) with the emphasis on practical limits and SoC implementation issues will follow. The impact of the continuously shrinking technologies on the usefulness of DFT in mixed signal environment is discussed. The tutorial concludes with a summary of open research problems and future directions in the mixed-signal DFT area.

PRESENTERS:

Bozena Kaminska - *3rd Millennium Test Solutions,
Lake Oswego, OR*
Karim Arabi - *PMC-Sierra, Vancouver, BC, Canada*

Time: 10:30 AM to 12:00 PM

Room: Pine/Fir

SESSION 9B EMBEDDED TUTORIAL: MANUFACTURING- AWARE PHYSICAL DESIGN

Moderators: Sani R. Nassif - *IBM Corp., Austin, TX*
Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

Ultra-deep submicron manufacturability impacts physical design (PD) through complex layout rules and large guardbands for process variability; this creates a requirement for new manufacturing-aware PD technologies. Part I of this tutorial reviews PD complications, and impact on methodology, arising from subwavelength lithography and deep-submicron manufacturing (antennas, metal planarization and mask-wafer mismatch). We define the cost of design in terms of catastrophic and parametric yield as well as mask NRE. Process variations and their sources are taxonomized for modeling and simulation. A framework of design for cost and value is described. Part II covers yield-constrained optimizations in PD, especially "beyond corners" approaches that escape today's pessimistic or even incorrect corner-based approaches. Statistical timing and noise analyses enable optimization of parametric yield and reliability. Yield-aware cell libraries and "analog" design rules (as opposed to "digital", 0/1 rules) can help designers explore yield-cost tradeoffs, especially for low-volume parts. Part III examines performance impact limited fill insertion which goes beyond mere capacitance rules. Modeling, objectives, and filling strategies (both grounded and floating) are discussed. Part IV gives an anatomy of design-to-manufacturing PD methodology. Key aspects include detailed routing technology, chip planning function, support for hard IP reuse, and integration with analysis and manufacturing interfaces. Part V gives futures for manufacturing-aware PD. This includes cost-benefit tradeoffs for "regular" layout structures that are likely beyond 90nm, cost optimizations for low-volume production, and the role of robust and/or stochastic optimization in PD.

PRESENTERS:

Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*
Puneet Gupta - *Univ. of California at San Diego, La Jolla, CA*

Time: 10:30 AM to 12:30 PM

Room: Donner/Siskiyou

SESSION 9C COOL TOPICS IN LOGIC SYNTHESIS

Moderators: Olivier R. Coudert - *Monterey Design Systems, Inc., Sunnyvale, CA*
Diana Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*

The first three papers address low power optimization. The first paper proposes a simple, fast heuristics to determine a low leakage sleep state input vector. The second one mixes multiple power supplies and voltage thresholds to achieve power efficient designs. The third one presents experiments about a low power FPGA flow. The fourth paper extends the concept of don't care to multi-valued networks.

9C.1 A HEURISTIC TO DETERMINE LOW LEAKAGE SLEEP STATE VECTORS FOR CMOS COMBINATIONAL CIRCUITS

Rahul M. Rao (rmrao@umich.edu) - *Univ. of Michigan, Ann Arbor, MI*
Frank Liu, Jeffrey L. Burns - *IBM Corp., Austin, TX*
Richard B. Brown - *Univ. of Michigan, Ann Arbor, MI*

9C.2 ALGORITHM FOR ACHIEVING MINIMUM ENERGY CONSUMPTION IN CMOS CIRCUITS USING MULTIPLE SUPPLY AND THRESHOLD VOLTAGES AT THE MODULE LEVEL

Yuvraj S. Dhillon (yuvraj@ece.gatech.edu), Abdulkadir U. Diril, Abhijit Chatterjee, Hsien-Hsin S. Lee - *Georgia Institute of Tech., Atlanta, GA*

9C.3 ON THE INTERACTION BETWEEN POWER-AWARE FPGA CAD ALGORITHMS

Julien Lamoureux (julient@ece.ubc.ca), Steven J.E. Wilton - *Univ. of British Columbia, Vancouver, BC, Canada*

9C.4 A THEORY OF NON-DETERMINISTIC NETWORKS

Alan Mishchenko, **Robert K. Brayton** (brayton@eecs.berkeley.edu) - *Univ. of California, Berkeley, CA*

Time: 10:30 AM to 12:30 PM

Room: Oak

SESSION 9D GRAPH ALGORITHMIC APPROACHES TO EDA PROBLEMS

Moderators: Dwight D. Hill - *Synopsys, Inc., Mountain View, CA*
Igor L. Markov - *Univ. of Michigan, Ann Arbor, MI*

This session covers a range of practical problems in EDA: partitioning, extraction, and the generation of parallel adders. While these areas are distinct, each of the papers in this session solves them by applying graph models. The partitioning papers define new metrics for quality: stability and subdomain degree. The synthesis paper defines a new approach to designing parallel adders. Finally, the extractor paper leverages cell library structures to improve gate recognition accuracy.

9D.1 STABLE MULTIWAY CIRCUIT PARTITIONING FOR ECO

Yongseok Cheon (cheon@cs.utexas.edu), Seokjin Lee - *Univ. of Texas, Austin, TX*
Martin D.F. Wong - *Univ. of Illinois, Urbana, IL*

9D.2 MULTI-OBJECTIVE HYPERGRAPH PARTITIONING ALGORITHMS FOR CUT AND MAXIMUM SUBDOMAIN DEGREE MINIMIZATION

Navaratnasothie Selvakumaran (selva@cs.umn.edu), George Karypis - *Univ. of Minnesota, Minneapolis, MN*

9D.3 AN ALGORITHMIC APPROACH FOR GENERIC PARALLEL ADDERS

Jianhua Liu (jhliu@cs.ucsd.edu), Shuo Zhou, Haikun Zhu, Chung-Kuan Cheng - *Univ. of California at San Diego, La Jolla, CA*

9D.4 FROSTY: A FAST HIERARCHY EXTRACTOR FOR INDUSTRIAL CMOS CIRCUITS

Lei Yang (yanglei@u.washington.edu), C.-J. Richard Shi - *Univ. of Washington, Seattle, WA*

Time: 2:00 PM to 4:00 PM

Room: Cedar

SESSION 10A PARAMETRIC CONSIDERATIONS IN TEST SCHEMES

Moderators: Andre Ivanov - *Univ. of British Columbia, Vancouver, BC, Canada*
Kwang-Ting (Tim) Cheng - *Univ. of California, Santa Barbara, CA*

In the attempt to improve test coverage the new techniques emerge which add different parametric effect modelling and analysis. Path delay is the one determining performance of high speed circuits. Two papers deal with the improved algorithms showing efficient new problem formulation and promising results. Static verification consideration and various noise sources analysis complete the session.

- 10A.1 PATH DELAY ESTIMATION USING POWER SUPPLY TRANSIENT SIGNALS: A COMPARATIVE STUDY USING FOURIER AND WAVELET ANALYSIS
Abhishek Singh, Jitin K. Tharian, Jim Plusquellic (plusquel@cs.umbc.edu) - *Univ. of Maryland, Baltimore, MD*
- 10A.2 LAYOUT-AWARE SCAN CHAIN SYNTHESIS FOR IMPROVED PATH DELAY FAULT COVERAGE
Puneet Gupta, Andrew B. Kahng, Ion I. Mandoiu, **Puneet Sharma** (sharma@vlsicad.ucsd.edu) - *Univ. of California at San Diego, La Jolla, CA*
- 10A.3 STATIC VERIFICATION OF TEST VECTORS FOR IR DROP FAILURE
Aman A. Kokrady, **C.P. Ravikumar** (ravikumar@ti.com) - *Texas Instruments, Bangalore, India*
- 10A.4 ATPG FOR NOISE-INDUCED SWITCH FAILURES IN DOMINO LOGIC
Rahul Kundu (rahul.kundu@intel.com) - *Intel Corp., Folsom, CA*
Ronald D. Blanton - *Carnegie Mellon Univ., Pittsburgh, PA*

Time: 2:00 PM to 4:00 PM

Room: Pine/Fir

SESSION 10B POWER-GRID AND SUBSTRATE ANALYSIS

Moderators: Kenneth L. Shepard - *Columbia Univ., New York, NY*
David Blaauw - *Univ. of Michigan, Ann Arbor, MI*

This session considers techniques for substrate and power-ground noise analysis. The first paper describes a statistical methodology for verifying power-supply integrity in the presence of leakage current variability. The second paper considers an approach for modelling substrate and power-ground noise introduced by digital blocks. RLC modelling approaches for the power-grid and substrate are considered in the third paper. The fourth paper introduces a new simulation approach for transient analysis of circuits with strong parasitic coupling.

- 10B.1 STATISTICAL VERIFICATION OF POWER GRIDS CONSIDERING PROCESS-INDUCED LEAKAGE CURRENT VARIATIONS
Imad A. Ferzli, Farid N. Najm (f.najm@utoronto.ca) - *Univ. of Toronto, Toronto, ON, Canada*
- 10B.2 A METHODOLOGY FOR THE COMPUTATION OF AN UPPER BOUND ON NOISE CURRENT SPECTRUM OF CMOS SWITCHING ACTIVITY
Alessandra Nardi (nardi@eecs.berkeley.edu), Haibo Zeng, Joshua L. Garrett - *Univ. of California, Berkeley, CA*
Luca Daniel - *Massachusetts Institute of Tech., Cambridge, MA*
Alberto L. Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*
- 10B.3 SUPREME: SUBSTRATE AND POWER-DELIVERY RELUCTANCE-ENHANCED MACROMODEL EVALUATION
Tsung Hao Chen (tchen@cae.wisc.edu), Clement Luk - *Univ. of Wisconsin, Madison, WI*
Charlie Chung-Ping Chen - *National Taiwan Univ., Taipei, Taiwan*
- 10B.4 SILCA: FAST-YET-ACCURATE TIME-DOMAIN SIMULATION OF VLSI CIRCUITS WITH STRONG PARASITIC COUPLING EFFECTS
Zhao Li (lz2000@u.washington.edu), C.-J. Richard Shi - *Univ. of Washington, Seattle, WA*

Time: 2:00 PM to 4:00 PM

Room: Donner/Siskiyou

SESSION 10C HOT TOPICS IN LOGIC SYNTHESIS

Moderators: Michel Berkelaar - *Magma Design Automation, Inc., Eindhoven, The Netherlands*
Yusuke Matsunaga - *Kyushu Univ., Fukuoka, Japan*

The session is about several aspects of clock management. The first paper addresses skew management in the presence of multiple clock phases. The second paper mixes skew optimization and hold buffer insertion. The third paper proposes a retiming method which includes control on the number of flip-flops. The last paper introduces an ILP formulation for asynchronous circuit synthesis.

10C.1 MULTI-DOMAIN CLOCK SKEW SCHEDULING

Kaushik Ravindran (kaushikr@eecs.berkeley.edu) - *Univ. of California, Berkeley, CA*
Andreas Kuehlmann, Ellen M. Sentovich - *Cadence Berkeley Labs., Berkeley, CA*

10C.2 CLOCK PERIOD MINIMIZATION OF NON-ZERO CLOCK SKEW CIRCUITS

Shih-Hsu Huang (shhuang@cycu.edu.tw), Yow-Tyng Nieh - *Chung Yuan Christian Univ., Chung Li, Taiwan*

10C.3 MINIMUM-AREA SEQUENTIAL BUDGETING FOR FPGA

Chao-Yang Yeh (cyeh@ece.ucsb.edu), Malgorzata Marek-Sadowska - *Univ. of California at Santa Barbara, Goleta, CA*

10C.4 ILP MODELS FOR THE SYNTHESIS OF ASYNCHRONOUS CONTROL CIRCUITS

Josep Carmona (jcarmona@ac.upc.es), Jordi Cortadella - *Technical Univ. Catalunya, Barcelona, Spain*

Time: 2:00 PM to 4:00 PM

Room: Oak

SESSION 10D INTERCONNECT MODELING

Moderators: Nick van der Meijs - *Delft Univ. of Tech., Delft, The Netherlands*
Sharad Kapur - *Integrand Software, Inc., Hoboken, NJ*

This session presents four papers on interconnect modeling. The first paper uses a non-uniform segmentation for analysing multiconductor transmission lines. The second paper uses an new approach to generate two stable poles from a moment representation. The third paper presents a new surface integral formulation which allows for the use of layered media greens functions. The final paper describes an extension of the switch factor technique for RC analysis to RLC analysis.

10D.1 PASSIVE SYNTHESIS OF COMPACT FREQUENCY-DEPENDENT INTERCONNECT MODELS VIA QUADRATURE SPECTRAL RULES

Traianos Yioultsis - *Aristotle Univ. of Thessaloniki, Thessaloniki, Greece*
Anne Woo, **Andreas C. Cangellaris** (cangella@uiuc.edu) - *Univ. of Illinois, Urbana, IL*

10D.2 ANALYTIC MODELING OF INTERCONNECTS FOR DEEP SUB-MICRON CIRCUITS

Dinesh Pamunuwa (dinesh@ele.kth.se) - *Royal Institute of Tech., Stockholm, Sweden*
Shauki Elassaad - *Cadence Design Systems, Inc., Berkeley, CA*
Hannu Tenhunen - *Royal Institute of Tech., Stockholm, Sweden*

10D.3 A NEW SURFACE INTEGRAL FORMULATION FOR WIDEBAND IMPEDANCE EXTRACTION OF 3-D STRUCTURES

Ben Song (bsong01@mit.edu), Zhenhai Z. Zhu - *Massachusetts Institute of Tech., Cambridge, MA*
John D. Rockway - *Lawrence Livermore National Lab., Livermore, CA*
Jacob K. White - *Massachusetts Institute of Tech., Cambridge, MA*

10D.4 SWITCH-FACTOR BASED LOOP RLC MODELING FOR EFFICIENT TIMING ANALYSIS

Yu Cao (ycao@eecs.berkeley.edu) - *Univ. of California, Berkeley, CA*
Xiaodong Yang - *Sun Microsystems, Sunnyvale, CA*
Xuejue Huang - *Rambus Inc., Los Altos, CA*
Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*

Time: 4:30 PM to 6:00 PM

Room: Cedar

SESSION 11A TEST DATA REDUCTION TECHNIQUES

Moderators: Alex Orailoglu - *Univ. of California at San Diego, La Jolla, CA*
Vivek Chickermane - *IBM Corp., Endicott, NY*

This session presents new ideas on coping with the increasing demands on automatic test equipment. Topics range from Scan vector compression and test response compaction to a new scheme for avoiding unnecessary yield reductions.

11A.1 ON COMPACTING TEST RESPONSE DATA CONTAINING UNKNOWN VALUES

Chen Wang (chen_wang@mentorg.com) - *Mentor Graphics Corp., Wilsonville, OR*

Sudhakar M. Reddy - *Univ. of Iowa, Iowa City, IA*

Irith Pomeranz - *Purdue Univ., West Lafayette, IN*

Janusz Rajski - *Mentor Graphics Corp., Wilsonville, OR*

Jerzy Tyszer - *Poznan Univ. of Tech., Poznan, Poland*

11A.2 ADJUSTABLE WIDTH LINEAR COMBINATIONAL SCAN VECTOR DECOMPRESSION

C.V. Krishna, Nur Touba (touba@ece.utexas.edu) - *Univ. of Texas, Austin, TX*

11A.3 ON APPLICATION OF OUTPUT MASKING TO UNDETECTABLE FAULTS IN SYNCHRONOUS SEQUENTIAL CIRCUITS WITH DESIGN-FOR-TESTABILITY LOGIC

Irith Pomeranz (pomeranz@ecn.purdue.edu) - *Purdue Univ., West Lafayette, IN*

Sudhakar M. Reddy - *Univ. of Iowa, Iowa City, IA*

Time: 4:30 PM to 6:00 PM

Room: Pine/Fir

SESSION 11B EMBEDDED TUTORIAL: FORMAL METHODS FOR DYNAMIC POWER MANAGEMENT

Moderators: Giovanni De Micheli - *Stanford Univ., Stanford, CA*
Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

Dynamic Power Management or DPM refers to the problem of judicious application of various low power techniques in an embedded system to minimize the total energy consumption. To be effective, often such decisions take into account the operating conditions and the system-level design goals. DPM has been a subject of intense research in the past decade driven by the need for low power in modern embedded devices. We present an overview of the formal methods that have been explored in solving the system-level DPM problem. We show how formal reasoning frameworks can unify apparently disparate DPM techniques. The first framework is based on the notion of competitive analysis of on-line algorithms. We survey various point solutions such as predictions based on regressions, exponential regression etc and show how competitive analysis of the problem can help devise near optimal DPM strategies. Next, we describe approaches that treat the DPM problem as one of stochastic optimization with probabilistic guarantees on performance. We survey stochastic DPM strategies and describe how probabilistic model checking can be used as a framework in which such strategies can be derived quite naturally. We conclude with an opinion on the research directions and problem generalization to include new technology capabilities such as dynamic speed scaling.

PRESENTERS:

Rajesh K. Gupta - *Univ. of California at San Diego, La Jolla, CA*

Sandeep Shukla - *Virginia Tech., Blacksburg, VA*

Sandy Irani - *Univ. of California, Irvine, CA*

Time: 4:30 PM to 6:00 PM

Room: Donner/Siskiyou

SESSION 11C EMBEDDED TUTORIAL: LARGE-SCALE CIRCUIT PLACEMENT: GAP AND PROMISE

Moderators: William H. Joyner, Jr. - SRC, Research Triangle Park, NC
Yoji Kajitani - Univ. of Kitakyushu, Fukuoka, Japan

Placement is one of the most important steps in the RTL to GDSII synthesis process, as it directly defines the interconnects, which have become the bottleneck in circuit and system performance in deep submicron technologies. The placement problem has been studied extensively in the past 30 years. However, recent studies showed that existing placement solutions are surprisingly far from optimal. The first part of this tutorial summarizes the results from the recent optimality and scalability studies of existing placement tools, which showed that the results of leading placement tools from both industry and academia are 50% to 150% away from the optimal solutions in terms of the total wirelength. If such a gap can be closed, it will be equivalent to several technology generation advancements. The second part of the tutorial highlights the recent progress on large-scale circuit placement, including techniques for wirelength minimization, routability optimization, and performance optimization. The last part of the tutorial discusses the placement problems for multi-million-gate FPGA designs, which have introduced special challenges and opportunities.

11C.1 EMBEDDED TUTORIAL: LARGE-SCALE CIRCUIT PLACEMENT: GAP AND PROMISE

Jason Cong (cong@cs.ucla.edu) - Univ. of California, Los Angeles, CA
Tim Kong - Magma Design Automation, Inc., Los Angeles, CA
Joseph R. Shinnerl, Min Xie, Xin Yuan - Univ. of California, Los Angeles, CA

11C.2 MULTI-MILLION GATE FPGA PHYSICAL DESIGN CHALLENGES

Salil Raje - Hier Design, Inc., Santa Clara, CA
Maogang Wang - Cadence Design Systems, Inc., San Jose, CA
Abhishek Ranjan - Hier Design, Inc., Santa Clara, CA

Time: 4:30 PM to 6:00 PM

Room: Oak

SESSION 11D STATISTICAL STATIC TIMING - II

Moderators: Nagib Z. Hakim - Intel Corp., Santa Clara, CA
Sani R. Nassif - IBM Corp., Austin, TX

Manufacturing induced timing variability has been recognized as one of the top new challenges for the DSM era. The papers in this session deal with the emerging area of statistical static timing analysis, a technique that holds promise in enabling the efficient incorporation of the impact of physical and environmental variability on overall design performance. This is an exciting emerging research area that will be the eventual interface between the integrated circuit manufacturing community and the timing signoff process.

11D.1 STATISTICAL TIMING ANALYSIS FOR INTRA-DIE PROCESS VARIATIONS WITH SPATIAL CORRELATIONS

Aseem Agarwal (abagarwa@umich.edu), David Blaauw - Univ. of Michigan, Ann Arbor, MI
Vladimir Zolotov - Motorola, Inc., Austin, TX

11D.2 A STATISTICAL GATE-DELAY MODEL CONSIDERING INTRA-GATE VARIABILITY

Kenichi Okada (okada@pi.titech.ac.jp), Kento Yamaoka, Hidetoshi Onodera - Kyoto Univ., Kyoto, Japan

11D.3 STATISTICAL CLOCK SKEW ANALYSIS CONSIDERING INTRA-DIE PROCESS VARIATION

Aseem Agarwal (abagarwa@umich.edu), David Blaauw - Univ. of Michigan, Ann Arbor, MI
Vladimir Zolotov - Motorola, Inc., Austin, TX

Tutorials9:00 AM - 5:00 PM
Continental Breakfast8:00 AM - 9:00 AM

Registration.....8:00 AM - 10:00 AM
Lunch12:00 PM - 1:00 PM

Cedar Ballroom

Tutorial 1 - Linux for EDA

Speakers: Stephen Edwards - *Columbia University, New York, NY*
Tom Grotton - *Cadence Design Systems, Inc., San Jose, CA*
Tim Marriott - *Synopsys, Inc., Santa Clara, CA*
Mel Nicholson - *Synopsys, Inc., Santa Clara, CA*
Fabio Somenzi - *Univ. of Colorado, Boulder, CO*

Over the last three years a large number of EDA tools have become available under Linux. While it is clear that the EDA industry has adopted Linux as one of the main platforms, the process of migrating applications to it has not reached maturity yet. This tutorial is therefore addressed to people involved in developing, porting, or deploying EDA software in the Linux environment. The tutorial will cover portability issues, programmer productivity tools, and performance analysis tools. The tutorial will also include a section on grid computing and the benefits and complexities of using parallel computing for CAD applications. Finally, the tutorial will include a discussion of the challenges involved in making Linux the main development platform.

The tutorial is intended for designers and CAD engineers interested in Linux as a CAD platform. Basic background in software development is useful though not needed.

Pine Ballroom

Tutorial 2- Leakage Issues in IC Design: Trends, Estimation and Avoidance

Speakers: Siva Narendra - *Intel Labs., Hillsboro, OR*
David Blaauw - *Univ of Michigan, Ann Arbor, MI*
Anirudh Devgan - *IBM Research, Austin, TX*
Farid Najm - *Univ. of Toronto, Toronto, ON, Canada*

Leakage power is emerging as a key challenge in IC design. Traditionally, leakage has been considered as an important design variable in handheld devices and in standby circuit operation. However, this significant increase of leakage now warrants that it be considered as the key design variable in all IC designs. This tutorial presents a comprehensive review of leakage power issues in IC design. The tutorial is organized in four major parts. The first part provides an overview of technology and scaling trends which are causing the significant increase in leakage current. The device physics that leads to sub-threshold and gate leakage will be described, along with their dependence on circuit design variables. The second part of the tutorial will focus on circuit level leakage estimation and avoidance. Comprehensive description of multiple-Vt techniques for leakage avoidance will be presented along with associated leakage estimation techniques. The third part of the tutorial focuses on chip level effects on leakage. Leakage estimation techniques which consider both inter and intra-die process variations will be covered as will leakage minimization techniques such as Adaptive Body Bias (ABB) and power supply control. The final part of the tutorial covers system and circuit architectures for leakage avoidance. In standby mode, the leakage of the circuit can be lowered by putting it a low-leakage state. This section of the tutorial will cover topics including state assignment for leakage minimization, leakage-driven memory and cache circuits and architectures.

The tutorial is intended for designers and CAD engineers interested in next generation design techniques and methodologies and emerging power challenges. Basic background of VLSI and CAD is useful though not needed.

Fir Ballroom

Tutorial 3- Recent Advances in Formal Verification

Speakers: Pei-Hsin Ho - *Synopsys, Inc., Beaverton, OR*
 Ken McMillan - *Cadence Berkeley Labs., Berkeley, CA*
 Vigyan Singhal - *Jasper Design Automation, Inc., Fremont, CA*

Recent progress in model checking techniques has allowed formal verification to be applied to larger and more complex design blocks. This tutorial will examine some of the recent methods that have led to a remarkable expansion in the capacity of formal verification tools. The tutorial will be divided into three parts. The first section will discuss iterative abstraction methods. One key to verifying assertions in larger designs is to be able to automatically determine which parts of a design are relevant to a given property. In the past few years, a number of new techniques have been developed for this purpose. This has made it possible in many cases to verify assertions on designs blocks with thousands of registers. The second portion will cover the role of Boolean SAT solvers in model checking. Many recent model checking approaches make use of Boolean satisfiability solvers. We will look at how SAT solvers work, why and in what cases they can be applied effectively to large problems, and how they can be exploited in model checking. The final section will cover predicate abstraction. This approach has made it possible to apply model checking to verify properties of relatively large pieces of software, such as device drivers in the Windows and Linux kernels.

The tutorial is intended for designers and CAD engineers interested in next generation formal verification methods. Basic background of VLSI and CAD is useful though not needed.

Oak Ballroom

Tutorial 4- Embedded Software Development

Speakers: Lance Brooks - *Mentor Graphics Corp., Mobile, AL*
 Mike McGrath - *Intel Corp., Chandler, AZ*
 Vladimir Ivanovic - *California State Univ., Hayward, CA*

Embedded software development is unlike software development for desktop or network environments. It is unique not only because every embedded device serves a unique purpose, it is different due to the very nature of firmware being very close to specialized hardware. This tutorial will provide an overview of the various pieces involved to develop embedded applications in a cross-target environment, including: integrated development environments for creating the software; compilers and associated tools for building the software targeted for various embedded CPUs and System-on-Chips (SoCs); debuggers designed to debug software running on the many different types of embedded CPU cores; and finally the different types of debug connections to various target execution environments and actual embedded hardware. The tutorial will also cover the specific problems faced by designers writing software prior to the availability of hardware. Attendees will leave with a good understanding of various pieces and the roles they play so they are better prepared to develop embedded software.

The tutorial is intended for designers and CAD engineers interested in the design of embedded software. Basic background in software development and VLSI is useful though not needed.