

Thursday, November 11, 2004

ICCAD-2004

Tutorials9:00 AM - 5:00 PM
Continental Breakfast8:00 AM - 9:00 AM

Registration8:00 AM - 3:00 PM
Lunch12:30 PM - 1:30 PM

The ICCAD 2004 Tutorials are renewed both content-wise and format-wise. First of all, the content has a new flavor oriented towards industrial practice. The topics and speakers have been selected such that for each topic they combine both a theoretical introduction of existing and new techniques with ample demonstration of industrial usage of the presented methods and techniques. This makes the tutorials extremely interesting for practicing designers and/or EDA professionals. The format is also different. Each tutorial runs for a half day; attendees receive the full set of notes and they can combine any half-day morning tutorial with any half-day afternoon tutorial, depending on their interests.

Pine Ballroom 9:00 AM - 12:30 PM

Tutorial 1 - **Best Practices in Low-Power Design: Part 1 : Power Reduction Techniques**

Speakers: **Enrico Macii** - *Politecnico di Torino, Torino, Italy*
Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

Targeted Audience: Industrial design engineers and EDA professionals who want to learn about basic low-power design techniques that can be used in industrial practice.

Description: In the last decade, huge effort has been invested to come up with a wide range of design solutions that help in solving the power consumption problem for different types of electronic devices, components and systems. Some of those solutions turned out to be very practical and effective, thus finding a path into commercial products of a different nature. Other approaches, which sounded promising on paper, showed too many limitations for attracting the attention of real designers. The objective of this tutorial is to offer the attendees some well-established, yet innovative recipes for addressing the power problem in real life. The presentation will be structured into two half-day tutorials. The morning tutorial will describe basic techniques, applicable at different levels of abstraction, that have proven to hold great potential for power optimization in practical design environments. They range from RTL power management and clock-tree architecture design to memory and bus interface design. Also some of the latest solutions regarding frequency and voltage dynamic control, as well as solutions for leakage power management will be discussed.

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Fir Ballroom 9:00 AM - 12:30 PM **Oak Ballroom** 9:00 AM - 12:30 PM

Tutorial 2- Physical Design at 90 nm and Beyond

Speakers: Andrew B. Kahng - *Univ. of California, San Diego, La Jolla, CA*
Pete J. Osler - *IBM Corp., Essex Junction, VA*

Targeted Audience: Industrial design and layout engineers and EDA professionals who want to learn about physical design challenges and solutions in advanced nanometer CMOS process technologies.

Description: Process variations, leakage, and scalability of runtime and QOR present critical challenges to IC physical design at the 90 nm node and beyond. Many established paradigms, such as sequenced synthesis, place, and route flows, will have to be replaced by new physical design methodologies and tool paradigms. This tutorial will cover five key shifts at 90 nm and beyond. We will discuss necessary algorithmic and flow changes that underlie manufacturing-aware cell-based place-and-route methodologies. Next, we will discuss methods and infrastructure for statistical and parameterized static timing analysis. Then we will discuss the benefits and challenges of integrated routing/placement/synthesis. Next, we will discuss next-generation thermal and leakage power-centric analysis and optimization flows that respond to the power and leakage issues. Finally, a view is provided on the long-term methodological trends that will govern the evolution of physical design.

Tutorial 3- Signal Integrity and Reliability of Integrated Circuits: Practical Considerations at 130 nm and Below

Speakers: Kenneth Tseng - *Cadence Design Systems, Inc., San Jose, CA*
Syed M. Alam - *Freescale Semiconductors, Austin, TX*

Targeted Audience: Industrial design and layout engineers and EDA professionals who want to learn about signal integrity and reliability challenges and solutions in real practical designs.

Description: At 130 nm and below, ignoring signal integrity (SI) is a luxury no designer can afford. SI-related issues are showing up in silicon from high-performance custom designs to ASICs and even FPGA-based designs, resulting in costly respins and missed market window. Hence, every designer needs an awareness of signal integrity prevention, analysis and repair. The SI problem promises to become even more challenging at 90 nm and 65 nm. The fundamental scaling barrier of supply and threshold voltages have given rise to a multitude of design techniques trading off timing versus power, yet making noise much worse than before. Increasing SI problems call for better analysis techniques and tools. The first part of the tutorial will explore new techniques in coupling aggressor alignment and statistical analysis of crosstalk. New delay models and tools are needed to handle the multitude of supply voltages and operating temperatures in a design. The second part of the tutorial focuses on reliability problems in integrated circuits, with a focus on electromigration, which is the primary interconnect reliability concern in integrated circuits. Cu interconnects are still susceptible to electromigration-induced failure over time. First the physical mechanisms and failure modes due to the electromigration phenomenon in both Al and dual-damascene Cu technologies will be reviewed. The bulk of the tutorial will focus on design procedures and CAD methodologies for circuit-level reliability assessment. A hierarchical reliability analysis flow will be discussed that accounts for the distinct reliability characteristics in Cu technology. Finally, future reliability issues with Cu/low-k technology and non-blocking vias will be explored.

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Tutorial 4- Best Practices in Low-Power Design: Part 2 : Industrial Power Reduction Experiences

Speakers: Vivek De - *Intel Corp., Hillsboro, OR*
Roberto Zafalon - *STMicroelectronics, Agrate, Italy*

Targeted Audience: Industrial design engineers and EDA professionals who want to learn about basic low-power design techniques that can be used in industrial practice.

Description: Huge effort has been invested in the last decade to come up with a wide range of design solutions that help in solving the power consumption problem for different types of electronic devices, components and systems. Some of those solutions turned out to be very practical and effective, thus finding a path into commercial products of a different nature. Other approaches, that sounded promising on paper, showed too many limitations for attracting the attention of real designers. The objective of this tutorial is to offer the attendees some well-established, yet innovative recipes for addressing the power problem in real life. The presentation will be structured into two half-day tutorials. The afternoon tutorial will focus on real-practice industrial experiences in low-power design for state-of-the-art systems. Speakers from Intel and STMicroelectronics will report on the results obtained by the application of low-power techniques to proprietary designs covering different application domains (e.g. high-performance microprocessors, and hardware platforms for embedded multi-media processing). A good mix of theory, application examples and real-life results will make the presentation valuable to designers interested in increasing their skills in low-power design and looking for solutions usable in their next-day product development.

Tutorial 5- Challenges and Solutions in the Design of High-Frequency Global Clock Distributions

Speakers: Phillip Restle - *IBM Research, Yorktown Heights, NY*
Ken Shepard - *Columbia Univ., New York, NY*

Targeted Audience: Industrial design engineers and EDA professionals who want to learn about global clock distribution techniques in industrial practice.

Description: This tutorial will begin with an overview of techniques that have been used for the successful design and analysis of global clock distributions. Popular methods of clock distributions will be compared, including the strategy of a clock-grid driven by tunable trees used by many of IBM's recent microprocessors. Both the modeling and design of the wires in these systems is critical; interconnect analysis techniques based on PEEC modeling will be illustrated with current-voltage animations. Despite past successes, current techniques for global clock distribution (including trees, grids, and tree-driven grids) are facing increasing challenges in distributing low-skew and low-jitter clocks. Furthermore, the power dissipated by the clock network is becoming a very significant fraction of the total power demands of the chip. Resonant clocking techniques, which resonate the clock capacitance with on-chip inductance, promise to ease these constraints, making possible low-skew and low-jitter clock distributions at reduced power. The inductance can come from on-chip wires (in the form of traveling wave and standing wave clocks) or spiral inductor topologies embedded into the clock wiring network. Both oscillator and resonant load topologies can be employed. In the latter part of this tutorial, we will review resonant clock techniques and predict the future impact of the technology.

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Tutorial 6- What's New in Algorithms for CAD Since You Left School?

Speakers: Stephen Boyd - *Stanford Univ., Stanford, CA*
Sachin Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

Targeted Audience: EDA and circuit design engineers and researchers.

Description: This tutorial covers two recent topics that are applicable in many IC design and EDA tasks : convex optimization, focusing on geometric programming (GP), and random walk techniques for solving systems of equations.

After an overview of convex optimization and new efficient solution methods, the first focus is on GP, and a powerful extension called generalized geometric programming (GGP). After covering the basics of GP and GGP modeling, their use in digital and analog device sizing problems will be illustrated, including topics such as design over corners, joint electrical and physical design, and fitting functions or empirical data in a form compatible with GP.

The second topic is a new class of methods that solve systems of positive definite equations, not by the conventional direct or iterative methods, but by running a set of random walks on a circuit graph. These methods have been successfully used in applications including capacitance extraction, analyzing on-chip power grids, and checking electrostatic discharge (ESD) networks, and have large potential for many other EDA problems, and can give good tradeoffs between accuracy and runtime.

New @ ICCAD

Thursday tutorials have a brand new look! ICCAD has developed an attendee-friendly format where you can mix and match tutorials to meet your personal needs.

- Six 1/2 day sessions
- **ADDED BONUS: Notes to all sessions**
- **Includes Continental Breakfast, Lunch and Coffee Breaks**

Registration Fees:

IEEE/ACM Member: \$320

Non-Member: \$395.00

Student: \$220.00

Join us on Thursday!