

Monday, November 8, 2004

ICCAD-2004

Registration - 7:00 AM - 6:00 PM (Bayshore Foyer)

Continental Breakfast - 7:00 AM (Sierra/Cascade Ballroom)

Speakers' Breakfast - 7:30 AM (Monterey Room)

8:30 **Opening Session & Keynote Address: Problems or Opportunities? Beyond the 90 nm Frontier**
Peter Rickert, P.E. - TI Fellow, Director of Platform Technology Development, Application Specific Products, Texas Instruments

9:45 Coffee Break

	Donner/Siskiyou Ballroom	Oak Ballroom	Pine/Fir Ballroom	Cedar Ballroom
10:30	SESSION 1A	SESSION 1B	SESSION 1C	SESSION 1D
	Statistical Modeling and Optimization Methodologies	System-level Energy Management	Equivalence Verification	Advances in Interconnect Analysis
12:00				
12:30				

12:00 - 2:00 Lunch Break (Sierra/Cascade Ballroom)

	SESSION 2A	SESSION 2B	SESSION 2C
2:00	Soft Error Rate Analysis	Application Specific Memory and Processor Architecture Design Techniques	Embedded Tutorial: The Care & Feeding of Your Statistical Static Timer (Pine/Fir Ballroom)
3:30			

Coffee Break

	SESSION 3A	SESSION 3B	SESSION 3C	SESSION 3D
4:00	Crosstalk-Aware Timing and Noise Analysis	System Software Optimizations	New Directions in Verification	Algorithms and Modeling Techniques for Bio and Nano Technologies
6:00				

ICCAD Panel Reception 6:00 PM - 6:30 PM

MONDAY NIGHT PANEL: DIVINE FOR DOLLARS

6:30 PM - 8:00 PM (Pine/Fir Ballroom)

ICCAD-2004

Tuesday, November 9, 2004

Registration - 7:00 AM - 6:00 PM (Bayshore Foyer)

Continental Breakfast - 7:00 AM (Sierra/Cascade Ballroom)

Technology Fair - 10:00 AM - 7:00 PM (Bayshore Foyer)

Speakers' Breakfast - 7:30 AM (Monterey Room)

Donner/Siskiyou Ballroom	Oak Ballroom	Pine/Fir Ballroom	Cedar Ballroom	
SESSION 4A				8:30
SESSION 4B				
SESSION 4C				10:00
SESSION 4D				
Developments in Timing Analysis and Optimization	Energy Efficiency and Interconnect Design	Floorplanning for Advanced Technologies	Robust Design Tools	
Coffee Break				
SESSION 5A				10:30
SESSION 5B				
SESSION 5C				12:00
SESSION 5D				
Embedded Tutorial: Variability Impact on Design	Architectural Issues in System Synthesis	Integrated Placement Applications	Novel Directions in Logic Synthesis	
12:00 - 2:00 Lunch Break (Sierra/Cascade Ballroom)				
SESSION 6A				2:00
SESSION 6B				
SESSION 6C				3:30
SESSION 6D				
Embedded Tutorial: World-Level Methods in Formal Verification	Interconnect Coding and Optimization	Statistical Timing Methods	New Methods in Power Grid Analysis	
Coffee Break				
SESSION 7A				4:00
SESSION 7B				
SESSION 7C				6:00
SESSION 7D				
Advances in SAT-based Verification	Power and Layout-Driven Logic Optimization	Advances in Floorplanning and Placement	Programmable Fabrics for Structured Design	
6:00 PM - 7:00 PM ICCAD TECHNOLOGY FAIR RECEPTION (Sierra/Cascade Ballroom)				

Wednesday, November 10, 2004

ICCAD-2004

Registration - 7:00 AM - 6:00 PM (Bayshore Foyer) Continental Breakfast - 7:00 AM (Sierra/Cascade Ballroom) Speakers' Breakfast - 7:30 AM (Monterey Room)

	Donner/Siskiyou Ballroom	Oak Ballroom	Pine/Fir Ballroom	Cedar Ballroom
8:30	SESSION 8A	SESSION 8B	SESSION 8C	SESSION 8D
	New Issues in Clocking	Innovative Models/Methods in Analog and Digital Diagnosis	Estimation and Management of Design Metrics	Advanced Analog/RF Macromodeling and Simulation
10:00	Coffee Break			
10:30	SESSION 9A	SESSION 9B	SESSION 9C	SESSION 9D
	Estimation Techniques for Physical Design	Timing Model Validation and Efficient On-Chip Test Compression	Embedded Tutorial: Emerging Technologies on the Design-Manufacturing Interface	Optimization Techniques for FPGAs and Reconfigurability
12:00	12:00 - 2:00 Lunch Break (Sierra/Cascade Ballroom)			
12:30	12:00 - 2:00 Lunch Break (Sierra/Cascade Ballroom)			
2:00	SESSION 10A	SESSION 10B	SESSION 10C	SESSION 10D
	Innovative Methods in High-Level Design	Power Analysis and Optimization	Routing	Analog Sizing and Optimization
3:30	Coffee Break			
4:00	SESSION 11A	SESSION 11B	SESSION 11C	SESSION 11D
	Variational Analysis of Interconnects	Test Generation for New Fault Models and Circuits	Embedded Tutorial: How to Bridge the Abstraction Gap in System Level Modeling and Design?	Hierarchical Mixed-Signal Modeling and Design
5:30				

Closing Reception 5:30 PM - 6:30 PM • See you next year! November 6 - 10, 2005 sponsored by:



Tutorials9:00 AM - 5:00 PM
Continental Breakfast8:00 AM - 9:00 AM

Registration8:00 AM - 3:00 PM
Lunch12:30 PM - 1:30 PM

Morning Tutorials • 9:00 AM - 12:30 PM

Afternoon Tutorials • 1:30 PM - 5:00 PM

Tutorial 1 - Best Practices in Low-Power Design: Part 1 : Power Reduction Techniques

Speakers: Enrico Macii - Politecnico di Torino, Torino, Italy
Massoud Pedram - Univ. of Southern California, Los Angeles, CA

Tutorial 2 - Physical Design at 90 nm and Beyond

Speakers: Andrew B. Kahng - Univ. of California, San Diego, La Jolla, CA
Pete J. Osler - IBM Corp., Essex Junction, VA

Tutorial 3 - Signal Integrity and Reliability of Integrated Circuits: Practical Considerations at 130nm and Below

Speakers: Kenneth Tseng - Cadence Design Systems, Inc., San Jose, CA
Syed M. Alam - Massachusetts Institute of Tech., Cambridge, MA

Tutorial 4 - Best Practices in Low-Power Design: Part 2 : Industrial Power Reduction Experiences

Speakers: Vivek De - Intel Corp., Hillsboro, OR
Roberto Zafalon - STMicroelectronics, Agrate, Italy

Tutorial 5 - Challenges and Solutions in the Design of High-Frequency Global Clock Distributions

Speakers: Phillip Restle - IBM Research, Yorktown Heights, NY
Ken Shepard - Columbia Univ., New York, NY

Tutorial 6 - What's New in Algorithms for CAD Since You Left School ?

Speakers: Stephen Boyd - Stanford Univ., Stanford, CA
Sachin Sapatnekar - Univ. of Minnesota, Minneapolis, MN

ICCAD-2004

International Conference on Computer Aided Design

• November 7 - 11 • DoubleTree Hotel • San Jose, CA

Keynote Address

Monday November 8
8:30 AM - 9:45 AM
Pine/Fir Ballroom

Keynote: *Problems or Opportunities? Beyond the 90 nm Frontier*

*Peter Rickert, P.E. - TI Fellow, Director of Platform Technology Development,
Application Specific Products, Texas Instruments*

Continued technology advances in the next ten years are based on 1) continued performance improvement and cost reduction through Moore's Law scaling of feature size and 2) SoC integration of analog and RF functions. Radically more sophisticated EDA capabilities are required in order for the industry to achieve this technology entitlement. This talk projects technology trends and identifies some of the key challenges for the EDA industry.

Several key new trends in the product space are driving the need for additional innovation in the EDA tool space. Several specific examples will be reviewed, notably, System-on-Chip Integration, Power Management (both leakage and active power reduction) Integration, and multiple CPU cores on a single chip along with multi million gates per chip driving the need for a higher level of abstraction to improve designer efficiency. Intermingled with these is the need for multivariable optimization, to close all the design gaps simultaneously, for improved efficiencies. Each of these will be discussed in detail.

This is coupled with the 65 nm and beyond process technology specific challenges which are also driving the need for additional EDA innovation. Notably design rule complexity explosion, sub lithographic feature implementation tools (Reticle Enhancement Technology and Optical Proximity Correction), and increased process variation and worst case corner explosion, requiring need for statistical simulation tools up and down the design flow.

Only through quick interaction between engineers from the product and process domains, along with the tool developers as well as academia and research labs will these new required capabilities have a chance of intersecting the timelines required to be leveraged on the 65 nm and 45nm product platforms. This talk will also include areas which should be driven towards open, non-proprietary standards to improve the overall efficiency of design organizations across the industry, leveraging lessons learned from recent history.

Let's all address these gaps with innovative solutions and end the arguments over what the timeline is for the end of Moore's Law!

Bio: Peter Rickert, P.E., is a TI Fellow and currently responsible for Platform Technology Development for the Application Specific Products (ASP) organization at TI. He manages the cross-functional team which encompasses the definition, development, and deployment of TI's deep submicron System on a Chip process technologies, including the 90 nm, 65 nm, and the 45 nm platforms. In 2000, Rickert was elected a TI Fellow in recognition of his leadership of new technology introductions and ramp to productions. He has held multiple management roles across TI during his 24 year career, including assignments in Houston, France, and now Dallas. He is widely recognized for his broad technical leadership and knowledge in process technology, ASIC design, testing, and program management. Rickert received his Bachelor of Science degree in Electrical and Computer Engineering at Clarkson University in 1980. He became a Registered Professional Engineer in the state of Texas in 1992 and is a senior member of the IEEE.

International Conference on Computer Aided Design
Monday Panel / Opening Session

ICCAD-2004
International Conference on Computer Aided Design

MONDAY PANEL: DIVINE FOR DOLLARS

Time: 6:30 PM to 8:00 PM

Room: Pine/Fir Ballroom

Moderator: Steve Kang - *Univ. of California, Santa Cruz, CA*

Although EDA spending is a small portion of the semiconductor chip budget, EDA can enable significant advances in chip productivity and capability. Technologies such as physical verification, place and route, and synthesis have made fundamental changes in how chips are designed. The time periods between significant innovations are generally filled with incremental improvements in EDA tools that generally involve performance, capacity, flow or feature improvements. As an industry, EDA needs to seek innovative ways to deliver greater value to our customers. If EDA is unable to provide the semiconductor industry with increased value from its products, it will not share in the growth of the semiconductor business.

The EDA industry needs to look to a variety of sources to provide inspiration for innovations that can deliver new value to semiconductor design and manufacturing. Academia and semiconductor roadmaps are common sources of inspiration. This panel seeks to obtain insights from our customers, namely designers. We invited five specialists with a variety of design backgrounds to discuss the next EDA innovations they think can change the way chips are developed. The panelists will first present proposals for these innovations. Then the table is turned. After discussion with the audience, the panelists will decide and justify which proposal they would actually back if they were an investor. Select members of the audience will vote on the proposal that, in its opinion, will change the way chips are designed. Business plan development will be the responsibility of the audience members after the conference.

Panelists:

Seth Copen Goldstein - *Carnegie Mellon Univ., Pittsburgh, PA*

Mark McDermott - *AMCC, Austin, TX*

Borivoje Nikolic - *Univ. of California, Berkeley, CA*

Kris Pister - *Dust Networks, Berkeley, CA*

Steve Teig - *Tabula, Mountain View, CA*

ICCAD
technology fair

Visit the Technology Fair to meet with professionals in the field, see demonstrations of the latest products, and make contacts and connections for the future.

Featured companies:

- Applied Simulation Technology
- IC Manage, Inc.
- Magma Design Automation, Inc.
- Novas Software, Inc.
- Prolific, Inc.
- Sagantec
- Sigrity, Inc.
- Silicon Canvas, Inc.
- Springer
- Stone Pillar Technologies, Inc.
- Zenasis Technologies, Inc.

Monday, November 8, 2004

ICCAD-2004

Time: 10:30 to 12:00

Room: Donner/Siskiyou Ballroom

SESSION 1A STATISTICAL MODELING AND OPTIMIZATION METHODOLOGIES

Moderators: Duane S. Boning - Massachusetts Institute of Tech.,
Cambridge, MA
Sani R. Nassif - IBM Corp., Austin, TX

Demands for effective methods in statistical modeling and optimization continue to rise. A novel probability distribution estimation approach using moment matching is proposed. In the second paper, statistical models are developed and used to improve SRAM yield by cell sizing. In the final paper, gate sizing optimization is presented to reduce cross-talk while preserving timing constraints.

1A.1 BEST PAPER WINNER ASYMPTOTIC PROBABILITY EXTRACTION FOR NON-NORMAL DISTRIBUTIONS OF CIRCUIT PERFORMANCE

Xin Li (xinli@ece.cmu.edu), Jiayong Le, Padmini
Gopalakrishnan, Lawrence T. Pileggi - Carnegie Mellon Univ.,
Pittsburgh, PA

1A.2 STATISTICAL DESIGN AND OPTIMIZATION OF SRAM CELL FOR YIELD ENHANCEMENT

Saibal Mukhopadhyay (sm@ecn.purdue.edu), Hamid Mahmoodi
Meiamand, Kaushik Roy - Purdue Univ., West Lafayette, IN

1A.3 GATE SIZING FOR CROSSTALK REDUCTION UNDER TIMING CONSTRAINTS BY LAGRANGIAN RELAXATION

Debjit Sinha (debjit@ece.northwestern.edu), Hai Zhou -
Northwestern Univ., Evanston, IL

Time: 10:30 to 12:00

Room: Oak Ballroom

SESSION 1B SYSTEM-LEVEL ENERGY MANAGEMENT

Moderators: Elaheh Bozorgzadeh - Univ. of California, Irvine, CA
Paolo Ienne - Swiss Federal Institute of Tech., Lausanne,
Switzerland

Energy management, in its many forms, is becoming one of the fundamental issues in the design of embedded systems. The first paper proposes a technique for energy minimization based on optimizing operating-mode transition sequences instead of focusing on individual transitions. The second paper argues that, in real devices, the energy minimization problem can be dominated by the fixed components of power consumption. The last paper of the session observes that scaling supply voltage reduces the possibilities of recovery and therefore addresses the trade-offs between system reliability and energy consumption.

1B.1 OPTIMIZING MODE TRANSITION SEQUENCES IN IDLE INTERVALS FOR COMPONENT-LEVEL AND SYSTEM-LEVEL ENERGY MINIMIZATION

Jinfeng Liu (jinfengl@ece.uci.edu), Pai H. Chou - Univ. of
California, Irvine, CA

1B.2 DYNAMIC VOLTAGE AND FREQUENCY SCALING UNDER A PRECISE ENERGY MODEL CONSIDERING VARIABLE AND FIXED COMPONENTS OF THE SYSTEM POWER DISSIPATION

Kihwan Cho (kihwancho@usc.edu), Wonbok Lee, Ramakrishna
Soma, Massoud Pedram - Univ. of Southern California, Los
Angeles, CA

1B.3 THE EFFECTS OF ENERGY MANAGEMENT ON RELIABILITY IN REAL- TIME EMBEDDED SYSTEMS

Dakai Zhu (zdk@cs.pitt.edu), Rami Melhem, Daniel Mosse -
Univ. of Pittsburgh, Pittsburgh, PA

ICCAD-2004

Time: 10:30 to 12:30

Room: Pine/Fir Ballroom

SESSION 1C EQUIVALENCE VERIFICATION

Moderators: Hanna Ziyad - Intel Corp., Haifa, Israel
Carl Pixley - Synopsys, Inc., Hillsboro, OR

Equivalence of circuits and subcircuits is an important verification problem and at the same time enables optimization of the representation. Equivalences may rely on contexts of design constraints and dynamic behavior. This session exposes these contexts and opportunities.

- 1C.1 **DAG-AWARE CIRCUIT COMPRESSION FOR FORMAL VERIFICATION**
Per M. Bjesse (bjesse@synopsys.com) - Synopsys, Inc., Hillsboro, OR
Arne Boraelv - Prover Technology Inc., Burlingame, CA
- 1C.2 **DYNAMIC TRANSITION RELATION SIMPLIFICATION FOR BOUNDED PROPERTY CHECKING**
Andreas Kuehlmann (kuehl@cadence.com) - Cadence Berkeley Labs., Berkeley, CA
- 1C.3 **THEORETICAL FRAMEWORK FOR COMPOSITIONAL SEQUENTIAL HARDWARE EQUIVALENCE VERIFICATION IN PRESENCE OF DESIGN CONSTRAINTS**
Zurab Khasidashvili (zurab.khasidashvili@intel.com) - Intel Corp., Haifa, Israel
- 1C.4 **CHECKING CONSISTENCY OF C AND VERILOG USING PREDICATE ABSTRACTION AND INDUCTION**
Daniel Kroening (kroening@cs.cmu.edu), Edmund Clarke - Carnegie Mellon Univ., Pittsburgh, PA

Monday, November 8, 2004

Time: 10:30 to 12:30

Room: Cedar Ballroom

SESSION 1D ADVANCES IN INTERCONNECT ANALYSIS

Moderators: Sharad Kapur - Integrand Software, Hoboken, NJ
Joel R. Phillips - Cadence Berkeley Labs, San Jose, CA

This session features innovations in interconnect simulation techniques. The first two papers present advances in application of model order reduction algorithms to RLC circuits by exploiting second-order system structure. The second pair of papers presents techniques for efficient modeling and simulation of large interconnect structures, including those with large numbers of terminals.

- 1D.1 **SAPOR: SECOND-ORDER ARNOLDI METHOD FOR PASSIVE ORDER REDUCTION OF RCS CIRCUITS**
Yangfeng Su, Jian Wang, Xuan Zeng (xzeng@fudan.edu.cn) - Fudan Univ., Shanghai, China
Zhaojun Bai - Univ. of California, Davis, CA
Dian Zhou - Fudan Univ., Shanghai, China
Charles Chiang - Synopsys, Inc., Mountain View, CA
- 1D.2 **BEST PAPER WINNER PRIM: STRUCTURE-PRESERVING REDUCED-ORDER INTERCONNECT MACROMODELING**
Roland W. Freund (freund@ucdavis.edu) - Univ. of California, Davis, CA
- 1D.3 **SPARSE AND EFFICIENT REDUCED ORDER MODELING OF LINEAR SUBCIRCUITS WITH LARGE NUMBER OF TERMINALS**
Peter Feldmann (feldmann@watson.ibm.com) - IBM Corp., Yorktown Heights, NY
Frank Liu - IBM Corp., Austin, TX
- 1D.4 **FAST SIMULATION OF VLSI INTERCONNECTS**
Jitesh Jain (jjain@purdue.edu), Cheng K. Koh, Venkataramanan R. Balakrishnan - Purdue Univ., West Lafayette, IN

Monday, November 8, 2004

ICCAD-2004

Time: 2:00 to 3:30

Room: Donner/Siskiyou Ballroom

SESSION 2A SOFT ERROR RATE ANALYSIS

Moderators: Duncan M. Walker - Texas A&M, College Station, TX
Louis Scheffer - Cadence Design Systems, Inc., San Jose, CA

Reduction in feature sizes has resulted in an increased sensitivity to random faults caused by radiation (single event upset). This is currently a problem for memories, and is going to become a problem for logic at the 45nm node. The papers in this session outline several algorithms for the analysis and reduction of the impact of SER.

2A.1 COST-EFFECTIVE RADIATION HARDENING TECHNIQUE FOR COMBINATIONAL LOGIC

Quming Zhou, Kartik Mohanram (kmram@rice.edu) - Rice Univ., Houston, TX

2A.2 IMPROVING SOFT-ERROR TOLERANCE OF FPGA CONFIGURATION BITS

Suresh Srinivasan, Aman Gayasen (gayasen@cse.psu.edu), Vijaykrishnan Narayanan, Mahmut Kandemir, Yuan Xie, Mary Jane Irwin - Penn State Univ., University Park, PA

2A.3 A SOFT ERROR RATE ANALYSIS (SERA) METHODOLOGY

Ming Zhang (mzhang2@uiuc.edu), Naresh R. Shanbhag - Univ. of Illinois, Urbana-Champaign, Urbana, IL

Time: 2:00 to 3:30

Room: Oak Ballroom

SESSION 2B APPLICATION SPECIFIC MEMORY AND PROCESSOR ARCHITECTURE DESIGN TECHNIQUES

Moderators: Nikil Dutt - Univ. of California, Irvine, CA
Hiroyuki Tomiyama - Nagoya Univ., Nagoya, Japan

This session focuses on optimization and simulation techniques for application specific embedded system components. The first paper presents a methodology for compiler-aided optimization of banked scratch-pad memories. The second paper presents a novel technique for application specific cache indexing. Finally, the last paper proposes a new approach to fast instruction-set simulation.

2B.1 BANKED SCRATCH-PAD MEMORY MANAGEMENT FOR REDUCING LEAKAGE ENERGY CONSUMPTION

Mahmut Kandemir (kandemir@cse.psu.edu), G. Chen, Mary Jane Irwin - Penn State Univ., University Park, PA
Ibrahim Kolcu - Univ. of Manchester, Manchester, UK

2B.2 REDUCING CACHE MISSES BY APPLICATION-SPECIFIC RE-CONFIGURABLE INDEXING

Kimish Patel - Politecnico di Torino, Torino, Italy
Luca Benini - Universita' di Bologna, Bologna, Italy
Enrico Macii - Politecnico di Torino, Torino, Italy
Massimo Poncino (massimo.poncino@univr.it) - Universita Di Verona, Verona, Italy

2B.3 DYNAMOSIM: A TRACE-BASED DYNAMIC COMPILED INSTRUCTION SET SIMULATOR

Wai Sum Mong, Jianwen Zhu (jzhu@eecg.toronto.edu) - Univ. of Toronto, Toronto, ON, Canada

ICCAD-2004

Time: 2:00 to 3:30

Room: Pine/Fir Ballroom

SESSION 2C EMBEDDED TUTORIAL: THE CARE AND FEEDING OF YOUR STATISTICAL STATIC TIMER

Moderators: Sachin Sapatnekar - Univ. of Minnesota, Minneapolis, MN

The recent rush to statistical static timing as a method for handling process variability has an Achilles Heel. Variability Characterization. Without robust accurate models of parameter variations within die, across a wafer, and from wafer to wafer, a statistical static timer is little better than more traditional corner-based simulation. The purpose of this tutorial is to make the attendees aware of these facts, of various other issues relating to the accuracy of models vs. hardware observations, and to show how special-purpose test structures can be used to create timing variability models that can then be used in a statistical static timing framework.

Presenters:

Sani Nassif (nassif@us.ibm.com) - IBM Corp., Austin, TX

Nagib Hakim (nagib.hakim@intel.com) - Intel Corp.,
Santa Clara, CA

Duane Boning (boning@mtl.mit.edu) - Massachusetts Institute of
Tech., Cambridge, MA

Monday, November 8, 2004

ICCAD-2004

Time: 4:00 to 6:00

Room: Donner/Siskiyou Ballroom

SESSION 3A CROSSTALK-AWARE TIMING AND NOISE ANALYSIS

Moderators: Charlie Chung-Ping Chen - National Taiwan Univ.,
Taipei, Taiwan
Noel Menezes - Intel Corp., Hillsboro, OR

Crosstalk analysis has reached an initial level of maturity in industry tools. The papers in this session highlight advances in crosstalk delay/noise analysis. The first paper proposes a novel Weibull-based approach to noise modeling. This is followed by a paper on comprehensive simulation-based noise-on-delay analysis flow. The third presentation deals with the unexplored area of crosstalk modeling for hierarchical IP blocks. A technique for reducing delay noise pessimism using logic techniques rounds out the session.

3A.1 ANALYTICAL MODELING OF CROSSTALK NOISE WAVEFORM WITH FOUR-PARAMETER WEIBULL FUNCTION

Alireza Kasnavi, Joddy W. Wang, Mahmoud Shahram (mahmouds@synopsys.com), Jindrich Zejda - Synopsys, Inc., Mountain View, CA

3A.2 ROBUST CELL-LEVEL CROSSTALK DELAY CHANGE ANALYSIS

Igor Keller (ikeller@cadence.com), Nishath Verghese, Kenneth Tseng - Cadence Design Systems, Inc., San Jose, CA

3A.3 TIMING MACROMODELING OF IP BLOCKS WITH CROSSTALK

Ruiming Chen (rui-chen@northwestern.edu), Hai Zhou - Northwestern Univ., Evanston, IL

3A.4 DELAY NOISE PESSIMISM REDUCTION BY LOGIC CORRELATIONS

Alexey Glebov, Sergey Gavrillov, Roman Soloviev - Microstyle, Moscow, Russia
Vladimir Zolotov - IBM T.J. Watson Research Center, Yorktown Heights, NY
Murat R. Becer (MuratBecer@motorola.com), Chanhee Oh, Rajendran Panda - Motorola, Inc., Austin, TX

Time: 4:00 to 6:00

Room: Oak Ballroom

SESSION 3B SYSTEM SOFTWARE OPTIMIZATIONS

Moderators: Wolfgang Nebel - Univ. of Oldenburg, Oldenburg, Germany
Joerg Henkel - Univ. of Karlsruhe, Karlsruhe, Germany

This session addresses code optimization techniques at various levels of abstraction covering algorithms, expressions, and instructions.

3B.1 FACTORING AND ELIMINATING COMMON SUBEXPRESSIONS IN POLYNOMIAL EXPRESSIONS

Anup Hosangadi (anup@ece.ucsb.edu) - Univ. of California, Santa Barbara, CA
Farzan Fallah - Fujitsu Labs. of America, Sunnyvale, CA
Ryan Kastner - Univ. of California, Santa Barbara, CA

3B.2 CUSTOM-OPTIMIZED MULTIPLIERLESS IMPLEMENTATIONS OF DSP ALGORITHMS

Markus P. eschel (pueschel@ece.cmu.edu), Adam Zelinski, James C. Hoe - Carnegie Mellon Univ., Pittsburgh, PA

3B.3 A QUANTITATIVE STUDY AND ESTIMATION MODELS FOR EXTENSIBLE INSTRUCTIONS IN EMBEDDED PROCESSORS

Newton Cheung (ncheung@cse.unsw.edu.au), Sri Parameswaran - Univ. of New South Wales, Sydney, Australia
Joerg Henkel - Univ. of Karlsruhe, Karlsruhe, Germany

3B.4 CODE PARTITIONING FOR SYNTHESIS OF EMBEDDED APPLICATIONS WITH PHANTOM

Andre Costi Nacul (nacul@ics.uci.edu), Tony Givargis - Univ. of California, Irvine, CA

ICCAD-2004

Time: 4:00 to 6:00

Room: Pine/Fir Ballroom

SESSION 3C NEW DIRECTIONS IN VERIFICATION

Moderators: Stuart Swan - Cadence Design Systems, Inc., Redwood City, CA
Daniel Kroening - Computer Systems Institute, ETH
Zuerich, Switzerland

One of the major challenges in formal verification is to present negative results in a way that is comprehensible to users and aids in diagnosis. This session presents two novel approaches to this problem, in different domains. Analog circuits also present a major challenge for formal methods. This session presents a successful application to nontrivial circuit. Finally, the promised performance benefits of accelerated simulation have been limited by the difficulty of accelerating the test bench. Here we see a new approach to eliminating this bottleneck.

3C.1 FORMAL VERIFICATION COVERAGE: COMPUTING THE COVERAGE GAP BETWEEN TEMPORAL SPECIFICATIONS

Sayantan Das, Prasenjit Basu, Ansuman Banerjee, Pallab Dasgupta (pallab@cse.iitkgp.ernet.in), Partha P. Chakrabarti - India Institute of Tech., Kharagpur, India
Chunduri R. Mohan - Intel Corp., Folsom, CA
Limor Fix, Roy Armoni - Intel Corp., Haifa, Israel

3C.2 DEBUGGING SEQUENTIAL CIRCUITS USING BOOLEAN SATISFIABILITY

Moayad Y. Fahim Ali, Andreas Veneris (veneris@eecg.toronto.edu), Sean A. Safarpour - Univ. of Toronto, Toronto, ON, Canada
Rolf Drechsler - Univ. of Bremen, Bremen, Germany
Alexander Smith - Univ. of Toronto, Toronto, ON, Canada
Magdy Abadir - Freescale Semiconductors, Inc., Austin, TX

3C.3 TOWARDS FORMAL VERIFICATION OF ANALOG DESIGNS

Smriti Gupta, Bruce H. Krogh, Rob A. Rutenbar (rutenbar@ece.cmu.edu) - Carnegie Mellon Univ., Pittsburgh, PA

3C.4 AUTOMATIC TRANSLATION OF BEHAVIORAL TESTBENCH FOR FULLY ACCELERATED SIMULATION

Young-Il Kim (zerone@vslab.kaist.ac.kr), Chong-Min Kyung - KAIST, Daejeon, Korea

Monday, November 8, 2004

Time: 4:00 to 6:00

Room: Cedar Ballroom

SESSION 3D ALGORITHMS AND MODELING TECHNIQUES FOR BIO AND NANO TECHNOLOGIES

Moderators: Andrew B. Kahng - Univ. of California, San Diego, La Jolla, CA
Sitaraman Iyer - Intel, Santa Clara, CA

The session starts with a pair of papers on biochip design which are followed by two papers on nanoscale interconnect. The first paper applies architectural synthesis to scheduling droplet flow in digital biochips. The second paper formulates the placement and routing problem for biochip design. The third paper presents a nanotube RLC model calling into question the use of nanotubes in high speed interconnect. The final paper presents a hybrid approach for electrostatic analysis of nanowires.

3D.1 ARCHITECTURAL-LEVEL SYNTHESIS OF DIGITAL MICROFLUIDICS-BASED BIOCHIPS

Fei Su (fs@ee.duke.edu), Krishnendu Chakrabarty - Duke Univ., Durham, NC

3D.2 SIMULTANEOUS DESIGN AND LAYOUT OF MULTIPLEXED CHEMICAL PROCESSING SYSTEMS ON MICROCHIPS

Anton J. Pfeiffer, Tamal Mukherjee, Steinar Hauan (hauan@cmu.edu) - Carnegie Mellon Univ., Pittsburgh, PA

3D.3 A CIRCUIT MODEL FOR CARBON NANOTUBE INTERCONNECTS: COMPARATIVE STUDY WITH CU INTERCONNECTS FOR SCALED TECHNOLOGIES

Arijit Raychowdhury (araycho@purdue.edu), Kaushik Roy - Purdue Univ., West Lafayette, IN

3D.4 HYBRID TECHNIQUES FOR ELECTROSTATIC ANALYSIS OF NANOWIRES

Gang Li, Narayan R. Aluru (aluru@uiuc.edu) - Univ. of Illinois, Urbana-Champaign, Urbana, IL

Tuesday, November 9, 2004

ICCAD-2004

Time: 8:30 to 10:00

Room: Donner/Siskiyou Ballroom

SESSION 4A DEVELOPMENTS IN TIMING ANALYSIS AND OPTIMIZATION

Moderators: David Overhauser - Cadence Design Systems, Inc., San Jose, CA
Tom Spyrou - Precision Software Development, Sunnyvale, CA

This session presents a selection of papers in timing analysis. The papers approach timing analysis at several levels ranging from linear and nonlinear timing techniques to system-level timing flow.

4A.1 COMPUTATION OF SIGNAL THRESHOLD CROSSING TIMES DIRECTLY FROM HIGHER ORDER MOMENTS

Yehea I. Ismail, Chirayu S. Amin (c-amin@northwestern.edu) - Northwestern Univ., Evanston, IL

4A.2 MODELING UNBUFFERED LATCHES FOR TIMING ANALYSIS

Chirayu S. Amin (c-amin@northwestern.edu) - Northwestern Univ., Evanston, IL
Florentin Dartu - Intel Corp., Hillsboro, OR
Yehea I. Ismail - Northwestern Univ., Evanston, IL

4A.3 A FLEXIBILITY AWARE BUDGETING FOR HIERARCHICAL FLOW TIMING CLOSURE

Olivier Omedes (omedes@cadence.com) - Cadence Design Systems, Inc., Valbonne, France
Michel Robert Lirimm - UMR CNRS Montpellier Ii, Montpellier, France
Mohamed Ramdani - ESEO Angers, Angers, France

Time: 8:30 to 10:00

Room: Oak Ballroom

SESSION 4B ENERGY EFFICIENCY AND INTERCONNECT DESIGN

Moderators: Engling Yeo - Univ. of California, Berkeley, CA
Thomas Burd - Consultant, Sunnyvale, CA

Novel design methods, particularly for energy-awareness, are of increasing importance in system design. The first paper extends voltage and frequency optimization to multiple devices in a system. The second paper optimizes power dissipation in latency-insensitive communication networks with FIFO relay stations. The third paper utilizes latches to improve the performance of traditional flop-based wire pipelines.

4B.1 ENERGY OPTIMIZATION FOR A TWO-DEVICE DATA FLOW CHAIN

Ravishankar Rao, Sarma Vrudhula (sarma@ece.arizona.edu) - Univ. of Arizona, Tucson, AZ

4B.2 A POWER AWARE SYSTEM LEVEL INTERCONNECT DESIGN METHODOLOGY FOR LATENCY-INSENSITIVE SYSTEMS

Vikas Chandra (vchandra@ece.cmu.edu) - Tabula Inc., Santa Clara, CA
Anthony Xu - Carnegie Mellon Univ., Pittsburgh, PA
Herman Schmit - Tabula Inc., Santa Clara, CA
Lawrence T. Pileggi - Carnegie Mellon Univ., Pittsburgh, PA

4B.3 EXPLOITING LEVEL SENSITIVE LATCHES IN WIRE PIPELINING

Vikram Seth - Texas A&M Univ., College Station, TX
Min Zhao - Freescale Inc., Austin, TX
Jiang Hu (jianghu@ee.tamu.edu) - Texas A&M Univ., College Station, TX

ICCAD-2004

Time: 8:30 to 10:00

Room: Pine/Fir Ballroom

SESSION 4C FLOORPLANNING FOR ADVANCED TECHNOLOGIES

Moderators: Igor L. Markov - Univ. of Michigan, Ann Arbor, MI
Deshanad Singh - Altera, Toronto, ON, Canada

Floorplanning is critical for new technologies. This session presents new floorplan techniques for advanced technologies. The first paper applies slicing techniques to heterogeneous multi-million gate FPGAs. The second paper proposes a new representation and algorithm for simultaneously floorplanning and scheduling reconfigurable integrated circuits. The last paper deals with thermal-driven floorplanning for 3D ICs.

- 4C.1 FLOORPLAN DESIGN FOR MULTI-MILLION GATE FPGAs
Lei Cheng (lcheng1@uiuc.edu), Martin DF Wong - Univ. of Illinois, Urbana-Champaign, Urbana, IL
- 4C.2 TEMPORAL FLOORPLANNING USING THE T-TREE FORMULATION
Ping Hung Yuh, Chia Lin Yang, Yao-Wen Chang (ywchang@cc.ee.ntu.edu.tw) - National Taiwan Univ., Taipei, Taiwan
- 4C.3 A THERMAL-DRIVEN FLOORPLANNING ALGORITHM FOR 3D ICs
Jason Cong, Jie Wei (jwei@cs.ucla.edu), Yan Zhang - Univ. of California, Los Angeles, CA

Tuesday, November 9, 2004

Time: 8:30 to 10:00

Room: Cedar Ballroom

SESSION 4D ROBUST DESIGN TOOLS

Moderators: Nagib Z. Hakim - Intel Corp., Santa Clara, CA
Haihua Su - IBM Corp., Austin, TX

The papers in this session focus on a number of chip-wide reliability problems that plague sub-100 nm designs. These include Electro-Static Discharge, Electromigration, and Thermal Reliability. The papers propose various simulation and analysis strategies for predicting the impact and mitigating the effects of these phenomena.

- 4D.1 A CHIP-LEVEL ELECTROSTATIC DISCHARGE SIMULATION STRATEGY
Haifeng Qian (qianhf@ece.umn.edu) - Univ. of Minnesota, Minneapolis, MN
Joseph N. Kozhaya - IBM Corp., Austin, TX
Sani R. Nassif - IBM Corp., Essex Junction, VT
Sachin S. Sapatnekar - Univ. of Minnesota, Minneapolis, MN
- 4D.2 EFFICIENT FULL-CHIP THERMAL MODELING AND ANALYSIS
Peng Li (pli@ece.cmu.edu) - Texas A&M Univ., College Station, TX
Lawrence T. Pileggi, Mehdi Asheghi - Carnegie Mellon Univ., Pittsburgh, PA
Rajit Chandra - Gradient Design Automation, Inc., Santa Clara, CA
- 4D.3 INTERCONNECT LIFETIME PREDICTION UNDER DYNAMIC STRESS FOR RELIABILITY-AWARE DESIGN
Zhijian Lu (zl4j@virginia.edu), Wei Huang, John Lach, Mircea Stan, Kevin Skadron - Univ. of Virginia, Charlottesville, VA

Tuesday, November 9, 2004

ICCAD-2004

Time: 10:30 to 12:00

Room: Donner/Siskiyou Ballroom

SESSION 5A EMBEDDED TUTORIAL: VARIABILITY IMPACT ON DESIGN

Moderator: Soha Hassoun - Tufts Univ., Medford, MA

With each semiconductor process node, the impact of environmental variations and semiconductor process variations become a larger portion of the cycle time of the product. Simply guardbanding for these effects leads to increased product development times and non-competitive products. This tutorial focuses on the impact of variations and how to manage design closure for ASICs, microprocessors, and SRAMs.

5A.1 PROCESS AND ENVIRONMENTAL VARIATION IMPACTS ON ASIC TIMING

Paul S. Zuchowski, Peter A. Habitz, Jerry D. Hayes, Jeffery H. Oppold - IBM Corp, Essex Junction, VT

5A.2 THE IMPACT OF DEVICE PARAMETER VARIATIONS ON THE FREQUENCY AND PERFORMANCE OF VLSI CHIPS

Samie B. Samaan - Intel Corp., Lake Oswego, OR

5A.3 VARIABILITY IN SUB-100NM SRAM DESIGNS

Ray Heald, Ping Wang - Sun Microsystems, Sunnyvale, CA

Time: 10:30 to 12:00

Room: Oak Ballroom

SESSION 5B ARCHITECTURAL ISSUES IN SYSTEM SYNTHESIS

Moderators: Tony Givargis - Univ. of California, Irvine, CA

Ryan Kastner - Univ. of California, Santa Barbara, CA

Architectural issues pose major challenges in system synthesis. As such, this session addresses relevant issues, e.g., memory sub-system design and optimization, on-chip communication, and low power design strategies under stringent timing constraints.

5B.1 APPLICATION-SPECIFIC BUFFER SPACE ALLOCATION FOR NETWORKS-ON-CHIP ROUTER DESIGN

Jingcao Hu, Radu Marculescu (radum@ece.cmu.edu) - Carnegie Mellon Univ., Pittsburgh, PA

5B.2 SIMULTANEOUS COMMUNICATION AND PROCESSOR VOLTAGE SCALING FOR DYNAMIC AND LEAKAGE ENERGY REDUCTION IN TIME-CONSTRAINED SYSTEMS

Alexandru Andrei (alean@ida.liu.se), Marcus T. Schmitz, Petru Eles, Zebo Peng - Linköping Univ., Linköping, Sweden
Bashir M. Al Hashimi - Univ. of Southampton, Southampton, UK

5B.3 HARDWARE/SOFTWARE MANAGED SCRATCHPAD MEMORY FOR EMBEDDED SYSTEM

Andhi Janapsatya (andhij@cse.unsw.edu.au), Sri Parameswaran, Aleksandar Ignjatovic - Univ. of New South Wales, Sydney, Australia

ICCAD-2004

Time: 10:30 to 12:30

Room: Pine/Fir Ballroom

SESSION 5C INTEGRATED PLACEMENT APPLICATIONS

Moderators: Hai Zhou - Northwestern Univ., Evanston, IL
Yao-Wen Chang - National Taiwan Univ., Taipei, Taiwan

This session deals with the integration of several circuit optimizations with placement. The first paper leverages retiming to improve circuit delay. Routability is considered in two papers, by means of whitespace allocation and reordering. The fourth paper seeks to mitigate crosstalk noise.

5C.1 PHYSICAL PLACEMENT DRIVEN BY SEQUENTIAL TIMING ANALYSIS

Aaron P. Hurst (ahurst@eecs.berkeley.edu) - Univ. of California, Berkeley, CA
Philip Chong, Andreas Kuehlmann - Cadence Berkeley Labs., Berkeley, CA

5C.2 ON INTERACTIONS BETWEEN ROUTING AND DETAILED PLACEMENT

Devang Jariwala (djariwal@glove.cs.uic.edu), John Lillis - Univ. of Illinois, Chicago, IL

5C.3 ROUTABILITY-DRIVEN PLACEMENT AND WHITE SPACE ALLOCATION

Chen Li (li35@ecn.purdue.edu) - Purdue Univ., West Lafayette, IN
Min Xie - Univ. of California, Los Angeles, CA
Cheng-Kok Koh - Purdue Univ., West Lafayette, IN
Jason Cong - Univ. of California, Los Angeles, CA
Patrick H. Madden - State Univ. of New York, Binghamton, NY

5C.4 TRUE CROSSTALK AWARE INCREMENTAL PLACEMENT WITH NOISE MAP

Haoxing Ren - IBM Corp., Austin, TX
David Pan (dpan@ece.utexas.edu) - Univ. of Texas, Austin, TX
Paul Villarrubia - IBM Corp., Austin, TX

Time: 10:30 to 12:30

Room: Cedar Ballroom

Tuesday, November 9, 2004

SESSION 5D NOVEL DIRECTIONS IN LOGIC SYNTHESIS

Moderators: Ankur Srivastava - Univ. of Maryland, College Park, MD
Elena V. Dubrova - Royal Institute of Tech., Stockholm, Sweden

This session presents new developments in various areas. The topics are cyclic combinational circuits, using a logical effort formulation in technology mapping, handling variability during gate sizing and an application of classical 2-level optimization to network routers.

5D.1 ON BREAKABLE CYCLIC DEFINITIONS

Jie-Hong R. Jiang (jiejiang@eecs.berkeley.edu), Alan Mishchenko, Robert K. Brayton - Univ. of California, Berkeley, CA

5D.2 LOGICAL EFFORT BASED TECHNOLOGY MAPPING

Shrirang K. Karandikar (srirang@ece.umn.edu), Sachin S. Sapatnekar - Univ. of Minnesota, Minneapolis, MN

5D.3 VARIABILITY INSPIRED IMPLEMENTATION SELECTION PROBLEM

Azadeh Davoodi, Ankur Srivastava (ankurs@glue.umd.edu), Vishal Khandelwal - Univ. of Maryland, College Park, MD

5D.4 M-TRIE: AN EFFICIENT APPROACH TO ON-CHIP LOGIC MINIMIZATION

Seraj Ahmed, Rabi Mahapatra (rabi@cs.tamu.edu) - Texas A&M Univ., College Station, TX

Tuesday, November 9, 2004

ICCAD-2004

Time: 2:00 to 3:30

Room: Donner/Siskiyou Ballroom

SESSION 6A EMBEDDED TUTORIAL: WORLD-LEVEL METHODS IN FORMAL VERIFICATION

Moderator: Ken McMillan - Cadence Design Systems, Inc., Berkeley, CA

6A.1 SYMBOLIC WORD-LEVEL HARDWARE VERIFICATION

Randal E. Bryant - Carnegie Mellon Univ., Pittsburgh, PA

Hardware designers have long followed the principle of separating data from control; this same separation can be applied to hardware verification, abstracting away the detailed representation and manipulation of the data in order to verify the overall correctness of the control logic. Rather than modeling words of data as collections of individual bits, symbolic word-level approaches represent words as symbolic values that can be stored in memories, passed along wires, and routed through multiplexors. Blocks that transform data, such as ALUs, are modeled using generic "uninterpreted" functions. These abstraction also enable verifying more general, parameterized model, where the correctness of an entire family of designs can be established.

6A.2 MODEL CHECKING, ABSTRACTION AND SYMBOLIC EXECUTION FOR SOFTWARE

Sriram K. Rajamani - Microsoft Research, Redmond, WA

Over the past few years, there has been growing interest in using techniques such as predicate abstraction, symbolic execution, model checking, and abstraction-refinement to prove properties about programs written in common programming languages like C. I will give an overview of the issues involved in applying these techniques to software, and also how compiler techniques such as data-flow analysis and pointer analysis interact with these techniques in building a usable verification system. Recent successes of these methods in operating system driver verification hold the promise of future applications to embedded software and system-level models.

Time: 2:00 to 3:30

Room: Oak Ballroom

SESSION 6B INTERCONNECT CODING AND OPTIMIZATION

Moderators: Rhett Davis - North Carolina State Univ., Raleigh, NC
Borivoje Nikolic - Univ. of California, Berkeley, CA,

Robust, energy-efficient, and high-performance interconnect is of critical importance in system-on-chip design. The first paper in this session uses light-weight error detection for self-calibrating, reliable communication. The second paper addresses energy efficiency with a serialized, encoded communication protocol. The third paper describes a fast algorithmic approach to retiming SoC interconnect networks.

6B.1 SOFT SELF-SYNCHRONIZING CODES FOR SELF-CALIBRATING COMMUNICATION

Frederic Worm (frederic.worm@epfl.ch), Paolo lenne, Patrick Thiran - Swiss Federal Institute of Tech., Lausanne, Switzerland

6B.2 SILENT: SERIALIZED LOW ENERGY TRANSMISSION CODING FOR ON- CHIP INTERCONNECTION NETWORKS

Kangmin Lee (kangmin@eeinfo.kaist.ac.kr), Sejoong Lee, HoiJun Yoo - KAIST, Daejeon, Korea

6B.3 OPTIMAL WIRE RETIMING WITHOUT BINARY SEARCH

Chuan Lin (chuanlin@northwestern.edu), Hai Zhou - Northwestern Univ., Evanston, IL

ICCAD-2004

Tuesday, November 9, 2004

Time: 2:00 to 3:30

Room: Pine/Fir Ballroom

SESSION 6C STATISTICAL TIMING METHODS

Moderators: Tom Spyrou - Precision Software Development,
Sunnyvale, CA
Yehea I. Ismail - Northwestern Univ., Evanston, IL

This session focuses on techniques for improving the accuracy of statistical timing analysis and its application to circuits with level sensitive latches.

6C.1 INTERVAL-VALUED REDUCED ORDER STATISTICAL INTERCONNECT MODELING

James Ma (jdma@ece.cmu.edu), Rob A. Rutenbar - Carnegie Mellon Univ., Pittsburgh, PA

6C.2 STATIC STATISTICAL TIMING ANALYSIS FOR LATCH-BASED PIPELINE DESIGNS

Chia-Tso Chao (mango@ece.ucsb.edu), Li Wang, Tim Cheng - Univ. of California, Santa Barbara, CA
Sandip Kundu - Intel Corp., Goleta, CA

6C.3 EFFICIENT STATISTICAL TIMING ANALYSIS THROUGH ERROR BUDGETING

Vishal Khandelwal (vishalk@eng.umd.edu), Ankur Srivastava, Azadeh Davoodi - Univ. of Maryland, College Park, MD

Time: 2:00 to 3:30

Room: Cedar Ballroom

SESSION 6D NEW METHODS IN POWER GRID ANALYSIS

Moderators: Chandramouli V. Kashyap - Flexlogics, Inc., Sunnyvale, CA
David Blaauw - Univ. of Michigan, Ann Arbor, MI

Power grid integrity has become a critical design issue. In this session, three novel approaches for power grid modeling and analysis are presented. The first paper presents a new method for worst-case power grid analysis based on extreme value statistics. The second paper introduces a method for simplifying the analysis of flip-chip designs using C4 locality considerations. The final paper presents a comprehensive hierarchical simulation framework for interconnect dominated circuits.

6D.1 VOLTAGE-DROP-CONSTRAINED OPTIMIZATION OF POWER DISTRIBUTION NETWORK BASED ON RELIABLE MAXIMUM CURRENT ESTIMATES

Nestoras Evmorfopoulos, Dimitris Karampatzakis, George Stamoulis (georges@uth.gr) - Univ. of Thessaly, Volos, Greece

6D.2 FAST FLIP-CHIP POWER GRID ANALYSIS VIA LOCALITY AND GRID SHELLS

Eli Chiprout (eli.chiprout@intel.com) - Intel Corp., Chandler, AZ

6D.3 HISIM: HIERARCHICAL INTERCONNECT-CENTRIC CIRCUIT SIMULATOR

Tsung Hao Chen - Synopsys, Inc., Taipei, Taiwan
Jeng Liang Tsai (jltsai@cae.wisc.edu) - Univ. of Wisconsin-Madison, Madison, WI
Charlie Chung Ping Chen - National Taiwan Univ., Taipei, Taiwan

Tuesday, November 9, 2004

ICCAD-2004

Time: 4:00 to 6:00

Room: Donner/Siskiyou Ballroom

SESSION 7A ADVANCES IN SAT-BASED VERIFICATION

Moderators: Ken McMillan - Cadence Design Systems, Inc., Berkeley, CA
Per Bjesse - Synopsys, Inc., Hillsboro, OR

SAT-based methods are leading-edge technology for scalable and efficient verification. The papers in this session present various novel ideas for performance improvements in different aspects of SAT-based verification.

7A.1 GUIDING CNF-SAT SEARCH VIA EFFICIENT CONSTRAINT PARTITIONING

Vijay Durairaj (durairaj@eng.utah.edu), Priyank Kalla - Univ. of Utah, Salt Lake City, UT

7A.2 INCREMENTAL DEDUCTIVE & INDUCTIVE REASONING FOR SAT-BASED BOUNDED MODEL CHECKING

Liang Zhang (liang@vt.edu) - Virginia Tech., Blacksburg, VA
Mukul R. Prasad - Fujitsu Labs of America, Inc., Sunnyvale, CA
Michael S. Hsiao - Virginia Tech., Blacksburg, VA

7A.3 EFFICIENT SAT-BASED UNBOUNDED SYMBOLIC MODEL CHECKING USING CIRCUIT COFACTORIZING

Malay Ganai (malay@nec-labs.com), Aarti Gupta, Pranav Ashar - NEC Labs America, Princeton, NJ

7A.4 EFFICIENT COMPUTATION OF SMALL ABSTRACTION REFINEMENTS

Bing Li (bli@colorado.edu), Fabio Somenzi - Univ. of Colorado, Boulder, CO

SESSION 7B POWER AND LAYOUT-DRIVEN LOGIC OPTIMIZATION

Moderators: Michel Berkelaar - Magma Design Automation, Inc., Eindhoven The Netherlands
Yusuke Matsunaga - Kyushu Univ., Kagus, Japan

The papers in this session present new ideas for leakage power optimization, maximum current estimation and layout-driven logic optimization.

7B.1 EXACT AND HEURISTIC APPROACHES TO INPUT VECTOR CONTROL FOR LEAKAGE POWER REDUCTION

Feng Gao (fgao@umich.edu), John P. Hayes - Univ. of Michigan, Ann Arbor, MI

7B.2 LEAKAGE CONTROL THROUGH FINE-GRAINED PLACEMENT AND SIZING OF SLEEP TRANSISTORS

Vishal Khandelwal (vishalk@eng.umd.edu), Ankur Srivastava - Univ. of Maryland, College Park, MD

7B.3 A VECTORLESS ESTIMATION OF MAXIMUM INSTANTANEOUS CURRENT FOR SEQUENTIAL CIRCUITS

Cheng Tao Hsieh, Jian Cheng Lin, Shih Chieh Chang (scchang@cs.nthu.edu.tw) - National Tsing Hua Univ., Hsinchu, Taiwan

7B.4 A NEW INCREMENTAL PLACEMENT ALGORITHM AND ITS APPLICATION TO CONGESTION-AWARE DIVISOR EXTRACTION

Satrajit Chatterjee (satrajit@cs.berkeley.edu), Robert K. Brayton - Univ. of California, Berkeley, CA

Time: 4:00 to 6:00

Room: Oak Ballroom

ICCAD-2004

Tuesday, November 9, 2004

Time: 4:00 to 6:00

Room: Pine/Flr Ballroom

SESSION 7C ADVANCES IN FLOORPLANNING AND PLACEMENT

Moderators: Dwight D. Hill - Synopsys, Inc., Mountain View, CA
Zhigang Pan - Univ. of Texas, Austin, TX

Floorplanning and placement have the biggest and most visible impact of any physical EDA activity. This session describes advances in block-level floorplanning, and techniques that combine floorplanning and gate-level placement to solve the "boulders and dust" problem.

7C.1 UNIFICATION OF PARTITIONING, PLACEMENT AND FLOORPLANNING

Saurabh N. Adya - Synplicity, Inc., Sunnyvale, CA
Shubhyant Chaturvedi - AMD, Austin, TX
Jarrod A. Roy, David A. Papa, Igor L. Markov
(imarkov@eecs.umich.edu) - Univ. of Michigan, Ann Arbor, MI

7C.2 MULTILEVEL EXPANSION-BASED VLSI PLACEMENT WITH BLOCKAGES

Bo Hu (hb@ece.ucsb.edu), Malgorzata Marek Sadowska - Univ. of California, Santa Barbara, CA

7C.3 AN ANALYTIC PLACER FOR MIXED-SIZE PLACEMENT AND TIMING-DRIVEN PLACEMENT

Andrew B. Kahng, Qinke Wang (qiwang@cs.ucsd.edu) - Univ. of California, San Diego, La Jolla, CA

7C.4 ENGINEERING DETAILS OF A STABLE FORCE-DIRECTED PLACER

Kristofer Vorwerk (kpvorwer@cheetah.vlsi.uwaterloo.ca),
Andrew Kennings, Anthony Vannelli - Univ. of Waterloo,
Waterloo, ON, Canada

Time: 4:00 to 6:00

Room: Cedar Ballroom

SESSION 7D PROGRAMMABLE FABRICS FOR STRUCTURED DESIGN

Moderators: Radu Marculescu - Carnegie Mellon Univ., Pittsburgh, PA
Tanay Karnik - Intel Corp., Hillsboro, OR

This session includes design methodologies for programmable gate arrays. The first two papers introduce novel design flows for metal and via programmable gate arrays to reduce the masks costs. The session also includes two papers on new techniques to minimize routing overhead in current FPGA architectures. They propose new routing circuitry and interconnect structures.

7D.1 AN INTEGRATED DESIGN FLOW FOR A VIA-CONFIGURABLE GATE ARRAY (VCGA)

Yajun Ran (ranyj@ece.ucsb.edu), Malgorzata Marek Sadowska - Univ. of California, Santa Barbara, CA

7D.2 A METAL AND VIA MASKSET PROGRAMMABLE VLSI DESIGN METHODOLOGY USING PLAs

Nikhil Jayakumar, Sunil P. Khatri (spkhatri@colorado.edu) - Univ. of Colorado, Boulder, CO

7D.3 ANALYSIS AND EVALUATION OF A HYBRID INTERCONNECT STRUCTURE FOR FPGAs

Renqiu Huang (huangr@eecs.uc.edu), Ranga Vemuri - Univ. of Cincinnati, Cincinnati, OH

7D.4 LOW-POWER PROGRAMMABLE ROUTING CIRCUITRY FOR FPGAs

Jason H. Anderson (janders@eecg.toronto.edu), Farid N. Najm - Univ. of Toronto, Toronto, ON, Canada

Wednesday, November 10, 2004

ICCAD-2004

Time: 8:30 to 10:00

Room: Donner/Siskiyou Ballroom

SESSION 8A NEW ISSUES IN CLOCKING

Moderators: Premal Buch - Magma Design Automation, Inc., Cupertino, CA
Weiping Shi - Texas A&M Univ., College Station, TX

This session includes three papers addressing various aspects of clocking method in ultra-deep submicron designs. The first paper proposes a methodology of statistical clock scheduling and post-silicon clock skew tuning. The second paper describes a clock schedule verification algorithm for latch based designs under process variations. The third paper introduces a novel technique for clock distribution and de-skewing.

8A.1 A YIELD IMPROVEMENT METHODOLOGY USING PRE- AND POST-SILICON STATISTICAL CLOCK SCHEDULING

Jeng-Liang Tsai (jltsai@cae.wisc.edu), DongHyun Baik - Univ. of Wisconsin, Madison, WI
Charlie Chung Ping Chen - National Taiwan Univ., Taipei, Taiwan
Kewal K. Saluja - Univ. of Wisconsin, Madison, WI

8A.2 CLOCK SCHEDULE VERIFICATION UNDER PROCESS VARIATIONS

Ruiming Chen (rui-chen@northwestern.edu), Hai Zhou - Northwestern Univ., Evanston, IL

8A.3 A NOVEL CLOCK DISTRIBUTION AND DYNAMIC DE-SKEWING METHODOLOGY

Arjun Kapoor, Nikhil Jayakumar - Univ. of Colorado, Boulder, CO
Sunil Khatri (sunil@ee.tamu.edu) - Texas A&M Univ., College Station, TX

Time: 8:30 to 10:00

Room: Oak Ballroom

SESSION 8B INNOVATIVE MODELS/METHODS IN ANALOG AND DIGITAL DIAGNOSIS

Moderators: Linda Milor - Georgia Institute of Tech., Atlanta, GA
Manuel d'Abreu - SUN Microsystems, Sunnyvale, CA

In this session new methods for diagnosing faults/defects in analog and digital circuits are discussed. Per-test fault diagnosis based method improves diagnostic resolution through innovative techniques while the X-fault model improves resolution based on defects. Analog diagnosis is based on small signal parameter extraction for process variations, modeling errors, and defects.

8B.1 ONE PER-TEST FAULT DIAGNOSIS USING THE X-FAULT MODEL

Xiaoqing Wen (wen@cse.kyutech.ac.jp), Tokiharu Miyoshi, Seiji Kajihara - Kyushu Institute of Tech, Iizuka, Japan
Laung Terng Wang - SynTest Technologies, Inc., Sunnyvale, CA
Kewal K. Saluja - Univ. of Wisconsin, Madison, WI
Kozo Kinoshita - Osaka Gakuin Univ., Suita, Japan

8B.2 DIAGNOSIS OF SMALL-SIGNAL PARAMETERS FOR BROADBAND AMPLIFIERS THROUGH S-PARAMETER MEASUREMENTS AND SENSITIVITY-GUIDED EVOLUTIONARY SEARCH

Fang Liu, Sule Ozev (sule@ee.duke.edu), Martin Brooke - Duke Univ., Durham, NC

8B.3 AN EFFICIENT METHOD FOR IMPROVING THE QUALITY OF PER-TEST FAULT DIAGNOSIS

Chunsheng Liu (chunshengliu@unlnotes.unl.edu) - Univ. of Nebraska, Lincoln, NE

ICCAD-2004

Wednesday, November 10, 2004

Time: 8:30 to 10:00

Room: Pine/Fir Ballroom

**SESSION 8C ESTIMATION AND MANAGEMENT OF
DESIGN METRICS**

Moderators: Seda Ogresci Memik - Northwestern Univ., Evanston, IL
Barry Pangrle - Synopsys, Inc., Mountain View, CA

Accurate estimation of design metrics and their efficient management during early stages of the design flow is crucial for generating high quality designs. The first paper in this session describes an algorithmic approach to time budgeting based on a min-cost flow formulation. The second paper presents an analytic technique for estimating the dynamic range of variables in non-linear systems. In the final paper, a methodology for rapid power estimation with accuracy close to RTL is described.

8C.1 A UNIFIED THEORY OF TIMING BUDGET MANAGEMENT

Elaheh Bozorgzadeh, Siddharth Choudhuri, Majid Sarrafzadeh - Univ. of California, Irvine, CA
Soheil Ghiasi (soheil@cs.ucla.edu) - Univ. of California, Los Angeles, CA

8C.2 DYNAMIC RANGE ESTIMATION FOR NONLINEAR SYSTEMS

Bin Wu, Jianwen Zhu, Farid N. Najm (f.najm@utoronto.ca) - Univ. of Toronto, Toronto, ON, Canada

8C.3 POWER ESTIMATION FOR CYCLE-ACCURATE FUNCTIONAL DESCRIPTIONS OF HARDWARE

Lin Zhong (lzhong@princeton.edu) - Princeton Univ., Princeton, NJ
Srivaths Ravi, Anand Raghunathan - NEC Labs America, Inc., Princeton, NJ
Niraj K. Jha - Princeton Univ., Princeton, NJ

Time: 8:30 to 10:00

Room: Cedar Ballroom

**SESSION 8D ADVANCED ANALOG/RF MACROMODELING
AND SIMULATION**

Moderators: Gu-Yeon Wei - Harvard Univ., Cambridge, MA
Joel R. Phillips - Cadence Berkeley Labs, San Jose, CA

The papers in this session present significant advances in analog/RF macromodeling and simulation. The first paper describes an innovative multi-grid-like preconditioner for harmonic balance based on an intuitive multi-level frequency decomposition technique. The session continues with a paper on a two-parameter homotopy technique applied to harmonic balance analysis of high-Q oscillators. The session ends with a paper on a novel and rigorous macromodeling algorithm and associated numerical techniques for oscillators that can be used for injection locking analysis of any kind of oscillator.

8D.1 EFFICIENT HARMONIC BALANCE SIMULATION USING MULTI-LEVEL FREQUENCY DECOMPOSITION

Peng Li (pli@ece.cmu.edu), Lawrence T. Pileggi - Carnegie Mellon Univ., Pittsburgh, PA

8D.2 FREQUENCY DOMAIN SIMULATION OF HIGH-Q OSCILLATORS WITH HOMOTOPY METHODS

Xiaochun Duan, Kartikeya Mayaram (karti@ece.orst.edu) - Oregon State Univ., Corvallis, OR

8D.3 AUTOMATED OSCILLATOR MACROMODELING TECHNIQUES FOR CAPTURING AMPLITUDE VARIATIONS AND INJECTION LOCKING

Xiaolue Lai (laixl@ece.umn.edu), Jaijeet Roychowdhury - Univ. of Minnesota, Minneapolis, MN

Wednesday, November 10, 2004

ICCAD-2004

Time: 10:30 to 12:00

Room: Donner/Siskiyou Ballroom

SESSION 9A ESTIMATION TECHNIQUES FOR PHYSICAL DESIGN

Moderators: Martin D.F. Wong - Univ. of Illinois, Urbana, IL
Hardy K. Leung - Magma Design Automation, Inc.,
Santa Clara, CA

This session presents several new ideas in estimation techniques, which are essential to solving very large-scale optimization problems in physical design. We start with two papers focusing on faster and more accurate wire-length estimation – the first adopts a constructive approach using fast table-lookup for small instances, and the second uses a combination of statistical and probabilistic techniques. The last paper presents a practical approach to estimate buffering delay for multi-pin nets in the presence of obstacles, promising both excellent runtime and high accuracy.

9A.1 FLUTE: FAST LOOKUP TABLE BASED WIRELENGTH ESTIMATION TECHNIQUE

Chris Chu (cnchu@iastate.edu) - Iowa State Univ., Ames, IA

9A.2 WIRE-LENGTH PREDICTION USING STATISTICAL PROBABILISTIC TECHNIQUES

Jennifer L. Wong (jwong@cs.ucla.edu) - Univ. of California, Los Angeles, CA

Azadeh Davoodi, Vishal Khandelwal, Ankur Srivastava - Univ. of Maryland, College Park, MD

Miodrag Potkonjak - Univ. of California, Los Angeles, CA

9A.3 ACCURATE ESTIMATION OF GLOBAL BUFFER DELAY WITHIN A FLOORPLAN

Charles Alpert - IBM Corp., Austin, TX

Jiang Hu - Texas A&M Univ., College Station, TX

Sachin Sapatnekar - Univ. of Minnesota, Minneapolis, MN

C.N. Sze (cnsze@ee.tamu.edu) - Texas A&M Univ., College Station, TX

Time: 10:30 to 12:00

Room: Oak Ballroom

SESSION 9B TIMING MODEL VALIDATION AND EFFICIENT ON-CHIP TEST COMPRESSION

Moderators: Martin Margala - Univ. of Rochester, Rochester, NY
Dan Saab - Case Western Reserve Univ., Cleveland, OH

In this session test compression/decompression techniques for efficient on-chip implementation and a method for timing validation based on post-silicon measurements are discussed. Proposed test decompression techniques aim at low overhead hardware implementation for decompression. Post-silicon timing validation is based on measurements on maximum delays associated with each test pattern.

9B.1 A PATH-BASED METHODOLOGY FOR POST-SILICON TIMING VALIDATION

Leonard Lee (lylee@ece.ucsb.edu), Li Wang, Tim Cheng - Univ. of California, Santa Barbara, CA
TM Mak - Intel Corp., Santa Clara, CA

9B.2 FRUGAL LINEAR NETWORK-BASED TEST DECOMPRESSION FOR DRASTIC TEST COST REDUCTIONS

Alex Orailoglu, Wenjing Rao, George Su (gpsu@ucsd.edu) - Univ. of California, San Diego, La Jolla, CA

9B.3 DESIGN SPACE EXPLORATION FOR AGGRESSIVE TEST COST REDUCTION IN CIRCULAR SCAN ARCHITECTURES

Baris Arslan (barslan@cs.ucsd.edu), Alex Orailoglu - Univ. of California, San Diego, La Jolla, CA

ICCAD-2004

Wednesday, November 10, 2004

Time: 10:30 to 12:30

Room: Pine/Fir Ballroom

**SESSION 9C EMBEDDED TUTORIAL:
EMERGING TECHNOLOGIES ON THE DESIGN
MANUFACTURING INTERFACE**

Moderator: Andreas Kuehlmann - Cadence Berkeley Labs, Berkeley, CA

9C.1 DESIGN/PROCESS LEARNING FROM ELECTRICAL TEST

Bernd Koenemann - Mentor Graphics Corp., San Jose, CA

Modern Design-For-Test (DFT) practices not only simplify test generation but also make it much easier to diagnose problems uncovered in electrical test. In fact, many diagnostics steps can be automated enough to enable batch processing of large quantities of fail data captured during production test. Hidden in these failed data is very valuable information about the product design, the manufacturing process, and interactions between the two. This embedded tutorial will provide an overview of some of the analysis methods that are being used and/or prototyped in the industry, as well as the underlying data sharing between design and manufacturing that is required for and enabled by the analyses.

9C.2 BACKEND CAD FLOWS FOR "RESTRICTIVE DESIGN RULES"

Mark Lavin, Fook-Luen Heng, Greg Northrup - IBM T.J. Watson Research Center, Yorktown Heights, NY

To meet challenges of "deep-subwavelength" technologies, lithography has come to rely increasingly on "data processes" such as shape fill, optical proximity correction, and RETs like altPSM. For emerging technologies (65nm and following) the computation cost and complexity of these techniques are themselves becoming bottlenecks in the Design-to-Silicon flow. This has motivated the recent calls for "restrictive design rules" such as fixed width/pitch/orientation of gate-forming polysilicon features. We have been exploring how the "Design Side" might take advantage of these restrictions, and will present some preliminary work on how we might reduce the computational cost throughout the back end of the design flow through the post-tapeout "data processes" while improving quality of results: the reliability of OPC/RET algorithms and the accuracy of models of manufactured products. We believe that the underlying technology, including simulation and analysis, may be applicable to a variety of approaches to Design For Manufacturability (DFM).

Time: 10:30 to 12:30

Room: Cedar Ballroom

**SESSION 9D OPTIMIZATION TECHNIQUES FOR FPGAS
AND RECONFIGURABILITY**

Moderators: James C. Hoe - Carnegie Mellon Univ., Pittsburgh, PA
Narendra V. Shenoy - Synopsys, Inc., Mountain View, CA

This session contains papers which consider optimizing various aspects of FPGAs.

**9D.1 HERMES: LUT FPGA TECHNOLOGY MAPPING ALGORITHM FOR
AREA MINIMIZATION WITH OPTIMUM DEPTH**

Maxim Teslenko, Elena V. Dubrova (elena@imit.kth.se) - Royal Institute of Tech., Stockholm, Sweden

**9D.2 DAOMAP: A DEPTH-OPTIMAL AREA OPTIMIZATION MAPPING
ALGORITHM FOR FPGA DESIGNS**

Deming Chen (demingc@cs.ucla.edu), Jason Cong - Univ. of California, Los Angeles, CA

**9D.3 VDD PROGRAMMABILITY TO REDUCE FPGA INTERCONNECT
POWER**

Fei Li (feil@ee.ucla.edu), Yan Lin, Lei He - - Univ. of California, Los Angeles, CA

**9D.4 CONFIGURATION BITSTREAM COMPRESSION FOR DYNAMICALLY
RECONFIGURABLE FPGAS**

Ju Hwa Pan, Tulika Mitra (tulika@comp.nus.edu.sg), Weng Fai Wong - National Univ. of Singapore, Singapore

Wednesday, November 10, 2004

ICCAD-2004

Time: 2:00 to 3:30

Room: Donner/Siskiyou Ballroom

SESSION 10A INNOVATIVE METHODS IN HIGH-LEVEL DESIGN

Moderators: Forrest D. Brewer - Univ. of California, Santa Barbara, CA
Michael Kishinevsky - Intel Corp., Hillsboro, OR

This session presents novel techniques for design at levels higher than RTL. The first paper describes a design exercise using a new design language called Bluespec and compares it to a classic RTL flow. The second paper proposes an automated method for integrating data-path elements into the memory subsystem design. In the third paper, an algorithm for carry-save optimization of arithmetic data-paths is described.

- 10A.1 **HIGH-LEVEL SYNTHESIS: AN ESSENTIAL INGREDIENT FOR DESIGNING COMPLEX ASICS**
Arvind (arvind@mit.edu) - Massachusetts Institute of Tech., Cambridge, MA
Rishiyur Nikhil - Bluespec, Waltham, MA
Daniel L. Rosenband, Nirav Dave - Massachusetts Institute of Tech., Cambridge, MA
- 10A.2 **HIGH-LEVEL SYNTHESIS USING COMPUTATION-UNIT INTEGRATED MEMORIES**
Niraj K. Jha, Chao Huang (chaoh@princeton.edu) - Princeton Univ., Princeton, NJ
Srivaths Ravi, Anand Raghunathan - NEC Laboratories America, Princeton, NJ
- 10A.3 **IMPROVED USE OF THE CARRY-SAVE REPRESENTATION FOR THE SYNTHESIS OF COMPLEX ARITHMETIC CIRCUITS**
Ajay K. Verma, Paolo lenne (Paolo.lenne@epfl.ch) - Swiss Federal Institute of Tech., Lausanne, Switzerland

Time: 2:00 to 3:30

Room: Oak Ballroom

SESSION 10B POWER ANALYSIS AND OPTIMIZATION

Moderators: David Overhauser - Cadence Design Systems, Inc., San Jose, CA
Rajendran Panda - FreeScale Semiconductor Inc., Austin, TX

This session presents several papers in the area of power analysis and optimization. The first paper addresses low-power bus design. The second paper examines low-power design considering process variation. The third paper discusses a new model for power grid voltage impact on timing.

- 10B.1 **FORMAL DERIVATION OF OPTIMAL ACTIVE SHIELDING FOR LOW-POWER ON-CHIP BUSES**
Maged M. Ghoneima (m_ghoneima@ieee.org), Yehea Ismail - Northwestern Univ., Evanston, IL
- 10B.2 **A GENERAL FRAMEWORK FOR PROBABILISTIC LOW-POWER DESIGN SPACE EXPLORATION CONSIDERING PROCESS VARIATION**
Ashish Srivastav (ansrivas@eecs.umich.edu), Dennis M. Sylvester - Univ. of Michigan, Ann Arbor, MI
- 10B.3 **TIMING ANALYSIS CONSIDERING SPATIAL POWER/GROUND LEVEL VARIATION**
Masanori Hashimoto (hasimoto@ist.osaka-u.ac.jp), Junji Yamaguchi, Hidetoshi Onodera - Kyoto Univ., Kyoto, Japan

ICCAD-2004

Wednesday, November 10, 2004

Time: 2:00 to 3:30

Room: Pine/Fir Ballroom

SESSION 10C ROUTING

Moderators: Hannah Yang - Intel Corp., Hillsboro, OR
Charles Chiang - Synopsys, Inc., Mountain View, CA

This session presents three papers on routing. The first paper gives an integrated approach to escape routing and layer assignment in high-performance packaging design. The second paper gives a provably good algorithm for bus routing. The last paper presents an FPGA routing system that can effectively meet short-path and long-path constraints.

10C.1 SIMULTANEOUS ESCAPE ROUTING AND LAYER ASSIGNMENT FOR DENSE PCBs

Muhammet M. Ozdal (ozdal@uiuc.edu), Martin DF Wong - Univ. of Illinois, Urbana-Champaign, Urbana, IL

10C.2 A PROVABLY GOOD ALGORITHM FOR HIGH PERFORMANCE BUS ROUTING

Muhammet M. Ozdal (ozdal@uiuc.edu), Martin DF Wong - Univ. of Illinois, Urbana-Champaign, Urbana, IL

10C.3 SIMULTANEOUS SHORT-PATH AND LONG-PATH TIMING OPTIMIZATION FOR FPGAS

Ryan Fung (rfung@altera.com), Vaughn Betz, William Chow - Altera Corp., Toronto, ON

Time: 2:00 to 3:30

Room: Cedar Ballroom

SESSION 10D ANALOG SIZING AND OPTIMIZATION

Moderators: Mar Hershenson - Sabio Labs., Palo Alto, CA
Jaijeet Roychowdhury - Univ. of Minnesota, Minneapolis, MN

This session presents advanced circuit-level sizing and optimization techniques. The first paper presents a new method for piecewise linear modeling of the feasibility regions of analog blocks and applies it to hierarchical sizing. The second paper presents a new sequential geometric programming technique with rank-one quadratic posynomial performance modeling. The third paper presents piecewise linear modeling techniques for geometric programming based optimization.

10D.1 ANALOG PERFORMANCE SPACE EXPLORATION BY FOURIER-MOTZKIN ELIMINATION WITH APPLICATION TO HIERARCHICAL SIZING

Guido Stehr (stehr@tum.de), Helmut Graeb, Kurt Antreich - Univ. of Munich, Munich, Germany

10D.2 ROBUST ANALOG/RF CIRCUIT DESIGN WITH PROJECTION-BASED POSYNOMIAL MODELING

Xin Li (xinli@ece.cmu.edu), Padmini Gopalakrishnan, Yang Xu, Lawrence T. Pileggi - Carnegie Mellon Univ., Pittsburgh, PA

10D.3 TECHNIQUES FOR IMPROVING THE ACCURACY OF GEOMETRIC-PROGRAMMING BASED ANALOG CIRCUIT DESIGN OPTIMIZATION

Jintae Kim (jintae@ee.ucla.edu), Jaeseo Lee, Lieven Vandenberghe, Chih Kong Ken Yang - Univ. of California, Los Angeles, CA

Wednesday, November 10, 2004

ICCAD-2004

Time: 4:00 to 5:30

Room: Donner/Siskiyou Ballroom

SESSION 11A VARIATIONAL ANALYSIS OF INTERCONNECTS

Moderators: Chung-Kuan Cheng - Univ. of California, San Diego, La Jolla, CA
Nick Van Der Meijs - Delft Univ. of Tech., Delft, The Netherlands

This session covers interconnect analysis with variations. The first paper proposes TBR projections based variational interconnect analysis. The second paper uses the Galerkin Approach to compute the stochastic response. The third paper derives the mean and variance of interconnect capacitance with random surface roughness.

11A.1 VARIATIONAL INTERCONNECT ANALYSIS VIA PMTBR

Joel R. Phillips (jrp@cadence.com) - Cadence Berkeley Labs., San Jose, CA

11A.2 STOCHASTIC ANALYSIS OF INTERCONNECT PERFORMANCE IN THE PRESENCE OF PROCESS VARIATIONS

Janet M. Wang, Praveen Ghanta (ghanta@email.arizona.edu), Sarma Vrudhula - Univ. of Arizona, Tucson, AZ

11A.3 A STOCHASTIC INTEGRAL EQUATION METHOD FOR MODELING THE ROUGH SURFACE EFFECT ON INTERCONNECT CAPACITANCE

Zhenhai Z. Zhu (zhzhu@mit.edu) - Massachusetts Institute of Tech., Cambridge, MA
Alper Demir - Koc Univ., Istanbul, Turkey
Jacob K. White - Massachusetts Institute of Tech., Cambridge, MA

Time: 4:00 to 5:30

Room: Oak Ballroom

SESSION 11B TEST GENERATION FOR NEW FAULT

MODELS AND CIRCUITS

Moderators: Bruce Cory - Nvidia, Santa Clara, CA
Annie Meixner - Intel Corp., Portland, OR

This session focuses on new test methods for emerging fault models and circuits. The papers introduce new test generation methods for transition faults for large industrial circuits, test generation for locally synchronous, globally asynchronous circuits, and efficient test methods based on the exploitation of multiple paths for FPGAs.

11B.1 DETECTION OF MULTIPLE TRANSITIONS IN DELAY FAULT TEST OF SPARC64 MICROPROCESSOR

Daisuke Maruyama, Akira Kanuma, Takashi Mochiyama, Hiroaki Komatsu, Yaroku Sugiyama, Noriyuki Ito (ito.noriyuki@jp.fujitsu.com) - Fujitsu Ltd., Kawasaki, Japan

11B.2 MINIMIZING THE NUMBER OF TEST CONFIGURATIONS FOR FPGAS

Erik V. Chmelar (echmelar@crc.stanford.edu) - Stanford Univ., Stanford, CA

11B.3 SPIN-TEST: AUTOMATIC TEST PATTERN GENERATION FOR SPEED-INDEPENDENT CIRCUITS

Feng Shi, Yiorgos Makris (yiorgos.makris@yale.edu) - Yale Univ., New Haven, CT

ICCAD-2004

Wednesday, November 10, 2004

Time: 4:00 to 5:30

Room: Pine/Fir Ballroom

**SESSION 11C EMBEDDED TUTORIAL: HOW TO BRIDGE
THE ABSTRACTION GAP IN SYSTEM
LEVEL MODELING AND DESIGN?**

Moderator: Wolfgang Rosenstiel - Univ. Of Tuebingen, Tuebingen,
Germany

As more and more processors and subsystems are integrated in a single system, the verification bottleneck is driving designers away from RTL and RTL-like strategies for verification and design to higher abstraction levels. Increasing system complexity, on the other hand, requires much faster simulation and analysis tools. This is leading to new standards and tools around transaction level modeling. Languages such as SystemC and SystemVerilog are rich in behavioral and structural constructs which enable modeling designs at different levels of abstraction without imposing a top-down or bottom-up design flow. In fact, most design flows are iterative and modules at different levels of abstractions have to be considered. A more abstract model is very useful to increase simulation speed and to improve formal verification. SystemC and SystemVerilog stress the importance of verification support for complex SoCs including improvement for hardware verification as well as for the verification of hardware dependent software. In today's design flows the software development can often only start after the hardware is available. This causes unacceptable delays for the software development. The idea of transaction level modeling (TLM) is to provide in an early phase of the hardware development transaction level models of the hardware. Based on these TLMs a fast enough simulation environment is the basis for the development of hardware and hardware dependent software. The presumption is to run these transaction level models at several tens or some hundreds of thousand transactions per second which should be fast enough for system level modeling and verification.

Presenters:

Arie Bernstein - Intel Corp., Petach-Tikva, Israel
Mark Burton - ARM, Inc., Cambridge, UK
Frank Ghenassia - STMicroelectronics, Crolles, France

Time: 4:00 to 5:30

Room: Cedar Ballroom

**SESSION 11D HIERARCHICAL MIXED-SIGNAL MODELING
AND DESIGN**

Moderators: Luis Miguel Silveira - Technical Univ. Lisboa,
Lisboa, Portugal
Ken Kundert - Cadence Design Systems, Inc., San Jose, CA

This session presents three papers that provide a hierarchical perspective on mixed-signal modeling and design. The first paper presents a comprehensive methodology that uses architectural-level power simulations to investigate software-dependent substrate noise influences on ADC performance. The second paper then introduces the concept of analog platforms to explore the design space of analog front-end circuitry. The final paper in this session introduces an adaptive sampling technique to model analog circuit performance parameters based on pseudo-cubic splines.

**11D.1 ANALYZING SOFTWARE INFLUENCES ON SUBSTRATE NOISE: AN
ADC PERSPECTIVE**

ByungTae Kang, Narayanan Vijaykrishnan, Mary Jane Irwin
(mji@cse.psu.edu) - Penn State Univ., University Park, PA

**11D.2 DESIGN SPACE EXPLORATION FOR A UMTS FRONT-END
EXPLOITING ANALOG PLATFORMS**

Fernando De Bernardinis (fdb@eecs.berkeley.edu) - Univ. of
California, Berkeley, CA

Simone Gambini, Federico Vincis - Univ. of Pisa, Pisa, Italy
Francesco Svelto, Rinaldo Castello - Univ. of Pavia,
Pavia, Italy

Alberto Sangiovanni Vincentelli - Univ. of California, Berkeley, CA

**11D.3 ADAPTIVE SAMPLING AND MODELING OF ANALOG CIRCUIT
PERFORMANCE PARAMETERS WITH PSEUDO-CUBIC SPLINES**

Glenn A. Wolfe (gwolfe@ececs.uc.edu), Ranga Vemuri - Univ.
of Cincinnati, Cincinnati, OH

Thursday, November 11, 2004

ICCAD-2004

Tutorials9:00 AM - 5:00 PM
Continental Breakfast8:00 AM - 9:00 AM

Registration.....8:00 AM - 3:00 PM
Lunch12:30 PM - 1:30 PM

The ICCAD 2004 Tutorials are renewed both content-wise and format-wise. First of all, the content has a new flavor oriented towards industrial practice. The topics and speakers have been selected such that for each topic they combine both a theoretical introduction of existing and new techniques with ample demonstration of industrial usage of the presented methods and techniques. This makes the tutorials extremely interesting for practicing designers and/or EDA professionals. The format is also different. Each tutorial runs for a half day; attendees receive the full set of notes and they can combine any half-day morning tutorial with any half-day afternoon tutorial, depending on their interests.

Pine Ballroom

9:00 AM - 12:30 PM

Tutorial 1 - Best Practices in Low-Power Design: Part 1 : Power Reduction Techniques

Speakers: Enrico Macii - *Politecnico di Torino, Torino, Italy*
Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

Targeted Audience: Industrial design engineers and EDA professionals who want to learn about basic low-power design techniques that can be used in industrial practice.

Description: In the last decade, huge effort has been invested to come up with a wide range of design solutions that help in solving the power consumption problem for different types of electronic devices, components and systems. Some of those solutions turned out to be very practical and effective, thus finding a path into commercial products of a different nature. Other approaches, which sounded promising on paper, showed too many limitations for attracting the attention of real designers. The objective of this tutorial is to offer the attendees some well-established, yet innovative recipes for addressing the power problem in real life. The presentation will be structured into two half-day tutorials. The morning tutorial will describe basic techniques, applicable at different levels of abstraction, that have proven to hold great potential for power optimization in practical design environments. They range from RTL power management and clock-tree architecture design to memory and bus interface design. Also some of the latest solutions regarding frequency and voltage dynamic control, as well as solutions for leakage power management will be discussed.

ICCAD-2004

Thursday, November 11, 2004

Tutorials9:00 AM - 5:00 PM
Continental Breakfast8:00 AM - 9:00 AM

Registration.....8:00 AM - 3:00 PM
Lunch12:30 PM - 1:30 PM

Fir Ballroom

9:00 AM - 12:30 PM

Oak Ballroom

9:00 AM - 12:30 PM

Tutorial 2- Physical Design at 90 nm and Beyond

Speakers: Andrew B. Kahng - *Univ. of California, San Diego, La Jolla, CA*
Pete J. Osler - *IBM Corp., Essex Junction, VA*

Targeted Audience: Industrial design and layout engineers and EDA professionals who want to learn about physical design challenges and solutions in advanced nanometer CMOS process technologies.

Description: Process variations, leakage, and scalability of runtime and QOR present critical challenges to IC physical design at the 90 nm node and beyond. Many established paradigms, such as sequenced synthesis, place, and route flows, will have to be replaced by new physical design methodologies and tool paradigms. This tutorial will cover five key shifts at 90 nm and beyond. We will discuss necessary algorithmic and flow changes that underlie manufacturing-aware cell-based place-and-route methodologies. Next, we will discuss methods and infrastructure for statistical and parameterized static timing analysis. Then we will discuss the benefits and challenges of integrated routing/placement/synthesis. Next, we will discuss next-generation thermal and leakage power-centric analysis and optimization flows that respond to the power and leakage issues. Finally, a view is provided on the long-term methodological trends that will govern the evolution of physical design.

Tutorial 3- Signal Integrity and Reliability of Integrated Circuits: Practical Considerations at 130 nm and Below

Speakers: Kenneth Tseng - *Cadence Design Systems, Inc., San Jose, CA*
Syed M. Alam - *Freescale Semiconductors, Austin, TX*

Targeted Audience: Industrial design and layout engineers and EDA professionals who want to learn about signal integrity and reliability challenges and solutions in real practical designs.

Description: At 130 nm and below, ignoring signal integrity (SI) is a luxury no designer can afford. SI-related issues are showing up in silicon from high-performance custom designs to ASICs and even FPGA-based designs, resulting in costly respins and missed market window. Hence, every designer needs an awareness of signal integrity prevention, analysis and repair. The SI problem promises to become even more challenging at 90 nm and 65 nm. The fundamental scaling barrier of supply and threshold voltages have given rise to a multitude of design techniques trading off timing versus power, yet making noise much worse than before. Increasing SI problems call for better analysis techniques and tools. The first part of the tutorial will explore new techniques in coupling aggressor alignment and statistical analysis of crosstalk. New delay models and tools are needed to handle the multitude of supply voltages and operating temperatures in a design. The second part of the tutorial focuses on reliability problems in integrated circuits, with a focus on electromigration, which is the primary interconnect reliability concern in integrated circuits. Cu interconnects are still susceptible to electromigration-induced failure over time. First the physical mechanisms and failure modes due to the electromigration phenomenon in both Al and dual-damascene Cu technologies will be reviewed. The bulk of the tutorial will focus on design procedures and CAD methodologies for circuit-level reliability assessment. A hierarchical reliability analysis flow will be discussed that accounts for the distinct reliability characteristics in Cu technology. Finally, future reliability issues with Cu/low-k technology and non-blocking vias will be explored.

Thursday, November 11, 2004

Tutorials9:00 AM - 5:00 PM
Continental Breakfast8:00 AM - 9:00 AM

Registration8:00 AM - 3:00 PM
Lunch12:30 PM - 1:30 PM

Pine Ballroom 1:30 PM - 5:00 PM

Fir Ballroom 1:30 PM - 5:00 PM

Tutorial 4- Best Practices in Low-Power Design: Part 2 : Industrial Power Reduction Experiences

Speakers: Vivek De - *Intel Corp., Hillsboro, OR*
Roberto Zafalon - *STMicroelectronics, Agrate, Italy*

Targeted Audience: Industrial design engineers and EDA professionals who want to learn about basic low-power design techniques that can be used in industrial practice.

Description: Huge effort has been invested in the last decade to come up with a wide range of design solutions that help in solving the power consumption problem for different types of electronic devices, components and systems. Some of those solutions turned out to be very practical and effective, thus finding a path into commercial products of a different nature. Other approaches, that sounded promising on paper, showed too many limitations for attracting the attention of real designers. The objective of this tutorial is to offer the attendees some well-established, yet innovative recipes for addressing the power problem in real life. The presentation will be structured into two half-day tutorials. The afternoon tutorial will focus on real-practice industrial experiences in low-power design for state-of-the-art systems. Speakers from Intel and STMicroelectronics will report on the results obtained by the application of low-power techniques to proprietary designs covering different application domains (e.g. high-performance microprocessors, and hardware platforms for embedded multi-media processing). A good mix of theory, application examples and real-life results will make the presentation valuable to designers interested in increasing their skills in low-power design and looking for solutions usable in their next-day product development.

Tutorial 5- Challenges and Solutions in the Design of High-Frequency Global Clock Distributions

Speakers: Phillip Restle - *IBM Research, Yorktown Heights, NY*
Ken Shepard - *Columbia Univ., New York, NY*

Targeted Audience: Industrial design engineers and EDA professionals who want to learn about global clock distribution techniques in industrial practice.

Description: This tutorial will begin with an overview of techniques that have been used for the successful design and analysis of global clock distributions. Popular methods of clock distributions will be compared, including the strategy of a clock-grid driven by tunable trees used by many of IBM's recent microprocessors. Both the modeling and design of the wires in these systems is critical; interconnect analysis techniques based on PEEC modeling will be illustrated with current-voltage animations. Despite past successes, current techniques for global clock distribution (including trees, grids, and tree-driven grids) are facing increasing challenges in distributing low-skew and low-jitter clocks. Furthermore, the power dissipated by the clock network is becoming a very significant fraction of the total power demands of the chip. Resonant clocking techniques, which resonate the clock capacitance with on-chip inductance, promise to ease these constraints, making possible low-skew and low-jitter clock distributions at reduced power. The inductance can come from on-chip wires (in the form of traveling wave and standing wave clocks) or spiral inductor topologies embedded into the clock wiring network. Both oscillator and resonant load topologies can be employed. In the latter part of this tutorial, we will review resonant clock techniques and predict the future impact of the technology.

Thursday, November 11, 2004

Tutorials9:00 AM - 5:00 PM
Continental Breakfast8:00 AM - 9:00 AM

Registration8:00 AM - 3:00 PM
Lunch12:30 PM - 1:30 PM

Oak Ballroom

1:30 PM - 5:00 PM

Tutorial 6- What's New in Algorithms for CAD Since You Left School?

Speakers: Stephen Boyd - *Stanford Univ., Stanford, CA*
Sachin Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

Targeted Audience: EDA and circuit design engineers and researchers.

Description: This tutorial covers two recent topics that are applicable in many IC design and EDA tasks : convex optimization, focusing on geometric programming (GP), and random walk techniques for solving systems of equations.

After an overview of convex optimization and new efficient solution methods, the first focus is on GP, and a powerful extension called generalized geometric programming (GGP). After covering the basics of GP and GGP modeling, their use in digital and analog device sizing problems will be illustrated, including topics such as design over corners, joint electrical and physical design, and fitting functions or empirical data in a form compatible with GP.

The second topic is a new class of methods that solve systems of positive definite equations, not by the conventional direct or iterative methods, but by running a set of random walks on a circuit graph. These methods have been successfully used in applications including capacitance extraction, analyzing on-chip power grids, and checking electrostatic discharge (ESD) networks, and have large potential for many other EDA problems, and can give good tradeoffs between accuracy and runtime.

New @ ICCAD

Thursday tutorials have a brand new look! ICCAD has developed an attendee-friendly format where you can mix and match tutorials to meet your personal needs.

- Six 1/2 day sessions
- **ADDED BONUS: Notes to all sessions**
- **Includes Continental Breakfast, Lunch and Coffee Breaks**

Registration Fees:

IEEE/ACM Member: \$320

Non-Member: \$395.00

Student: \$220.00

Join us on Thursday!